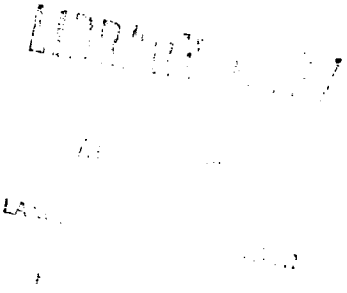

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N84-19705#

W-44362

FINAL REPORT

KA-BAND GaAs FET LOW NOISE RECEIVER/DEVICE DEVELOPMENT

1 DECEMBER 1979 THROUGH 1 MAY 1982
CONTRACT NO. NAS5-25968

PREPARED FOR

NATIONAL AERONAUTICAL & SPACE ADMINISTRATION
GODDARD SPACE FLIGHT CENTER
GREENBELT, MD 20771

NOVEMBER 1982

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SECURITY CLASSIFICATION OF THIS PAGE *(When Data Entered)*

REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER	2. GOVT ACCESSION NO.	3. RECIPIENT'S CATALOG NUMBER
4. TITLE *(and Subtitle)* Ka-Band GaAs FET Low Noise Receiver/Device Development		5. TYPE OF REPORT & PERIOD COVERED Final Technical Report 1 Dec. 1979 - 1 May 1982 6. PERFORMING ORG. REPORT NUMBER W44362
7. AUTHOR(s) J. M. Schellenberg, M. Feng, L. H. Hackett, E. T. Watkins and H. Yamasaki		8. CONTRACT OR GRANT NUMBER(s) NAS5-25968
9. PERFORMING ORGANIZATION NAME AND ADDRESS Hughes Aircraft Company, Torrance Research Center 3100 West Lomita Boulevard, P. O. Box 2999 Torrance, California 90509		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS
11. CONTROLLING OFFICE NAME AND ADDRESS NASA Goddard Space Flight Center Greenbelt Road Greenbelt, MD 20771		12. REPORT DATE October 1982 13. NUMBER OF PAGES 210
14. MONITORING AGENCY NAME & ADDRESS*(if different from Controlling Office)*		15. SECURITY CLASS. *(of this report)* Unclassified 15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT *(of this Report)*

Distribution limited to U.S. Government agencies only, test and evaluation, November 1982. Other requests for this document may be referred to NASA GSFC, Greenbelt, Maryland, Attn. code 727.

17. DISTRIBUTION STATEMENT *(of the abstract entered in Block 20, if different from Report)*

18. SUPPLEMENTARY NOTES

19. KEY WORDS *(Continue on reverse side if necessary and identify by block number)*

GaAs FET Devices
Low Noise Receiver
Millimeter Wave
Low Noise Amplifiers
Dual-Gate Mixers
FET Oscillators

20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

The objective of this program was to develop the technology for a 30 GHz low noise receiver utilizing GaAs FET devices exclusively. This program required advances in GaAs materials, devices and circuits. Specifically, we developed single and dual-gate FET devices, low noise FET amplifiers, dual-gate FET mixers and FET oscillators operating at Ka-band frequencies. As part of this program, a new 0.25 μm gate FET device was developed with a minimum noise figure of 3.3 dB at 29 GHz and an associated gain of 7.4 dB. Using this

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20. device, a 3-stage amplifier was fabricated with a minimum noise figure and associated gain of 4.4 dB and 17 dB, respectively. The 1-dB gain bandwidth of this amplifier extended from below 26.5 GHz to 30.5 GHz. In addition, a dual-gate mixer was demonstrated with a 2 dB conversion loss and a minimum noise figure of 10 dB at 29 GHz. A dielectric resonator stabilized FET oscillator was developed at 25 GHz for the receiver LO.

Using these FET components, a hybrid microwave integrated circuit receiver was constructed. This receiver demonstrated a minimum single-side band noise figure of 4.6 dB at 29 GHz with a conversion gain of 17 dB. The 1-dB noise bandwidth was 1.6 GHz while the 3-dB gain bandwidth was 1.4 GHz. The output power at the 1-dB gain compression point was -5 dBm. At the conclusion of the program, this FET receiver was delivered to NASA.

FOREWORD

This project was initiated by the NASA Goddard Space Flight Center with Mr. Chrissotimos, code 727, as the technical officer. This report summarizes the work performed from 1 December 1979 to 1 May 1982 under Contract No. NAS5-25968.

The work described herein was carried out at the Torrance Research Center, Electron Dynamics Division of Hughes Aircraft Company, Torrance, CA 90509. The program was directed by Mr. J.M. Schellenberg with Mr. E.T. Watkins as principal investigator.

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1.0 INTRODUCTION

This is the final report for the 18-month program, Ka-band GaAs FET Low Noise Receiver/Device Development, which was performed under Contract No. NAS5-25968. This is the first phase of a multiphase program to develop a 30 GHz low noise receiver utilizing GaAs FET technology exclusively. The objective of this first phase was to develop the key FET based components and demonstrate a hybrid microwave integrated circuit receiver utilizing these components. To realize this goal, significant advances were required in the state of the art of low noise FET devices for the RF preamplifier, dual-gate FET devices for the mixer and low 1/f noise FET devices for the local oscillator.

The GaAs FET is a versatile device that has been applied to low noise and power applications ranging in frequency from UHF to Ka-band. Never before has such a universal device hit the microwave industry. Recently, the FET has been pushing higher in frequency invading the realm of the IMPATT and Gunn diodes. It seems destined to rule the microwave spectrum from 1 to 100 GHz. The GaAs FET, as a 3-terminal device, is clearly superior to 2-terminal negative resistance devices in low noise amplifier applications. It is capable of lower noise amplification, possesses inherent input/output isolation, and is suitable for hybrid or monolithic MIC inclusion.

However, until recently, LN FET devices have been limited to frequencies below 20 GHz by poor noise performance and low gain. With the advent of improved gate lithography techniques, specifically, electron beam lithography, FET devices with 0.25 μm gate lengths have become available thereby extending the useful operating frequency range of FET devices to 40 GHz and beyond.[1]

During this program, we have developed single and dual-gate FET devices, low noise FET amplifiers, dual-gate FET mixers and FET oscillators operating at Ka-band frequencies. A summary of our accomplishments include:

- Development of a low noise 0.25 μm FET device with a minimum noise figure of 3.3 dB and an associated gain of 7.4 dB at 29 GHz.

- A three-stage FET LNA with a minimum noise figure of 4.4 dB and a gain of 17 dB.

- Dielectric resonator stabilized FET LO with an output power of 10 dBm at 25 GHz.

- Dual-gate FET mixer with a minimum conversion loss of 2 dB and a noise figure of 10 dB at 29 GHz.

- A FET receiver with a minimum noise figure of 4.6 dB with a conversion gain of 17 dB at 29 GHz.

The above results represent new state-of-the-art performance levels for FET devices and circuits. These results were achieved by a combined materials, devices and circuits effort.

2.0 GaAs MATERIALS

Our baseline materials approach for this program was vapor phase epitaxy (VPE) fabricated by the $AsCl_3/Ga/H_2$ process. For comparison, ion implantation (II) and liquid phase epitaxy (LPE) were also used to fabricate channel layers for FET devices. These technologies represent a wide range of channel layer formation methods. Based on the device performance results, we were able to assess the channel properties that are unique to each channel formation technology.

Active layers fabricated by II into VPE intrinsic buffer layers yielded low noise FETs with excellent RF performance, uniformity and reproducibility. This channel formation technique can minimize the influence of the semi-insulating substrate properties on the active channel layer. In contrast, direct implantation into semi-insulating substrates exhibited inconsistent channel properties which, in turn, produced inconsistent RF performance. High resistivity undoped high pressure liquid encapsulated Czochralski (LEC) wafers generally yielded more consistent and uniform properties for ion implantation than did the chromium doped horizontal Bridgeman (HB) wafers.

The LPE channel layers also have exhibited a large variation in device performance from wafer to wafer. The devices from "good" material yielded excellent performance at 30 GHz and above. An additional LPE channel problem, which is more serious in terms of device fabrication, is the nonuniformity of the layer over the wafer. Unless this nonuniformity problem is solved, LPE microwave devices will be limited mainly to experimental use.

VPE materials have consistently produced excellent device performance, particularly at frequencies above 20 GHz. One problem associated with the VPE layers was the lack of doping level uniformity and layer thickness. However, the recent introduction of round wafers to VPE reactors has significantly improved layer uniformity.

2.1 $AsCl_3/Ga/H_2$ VPE SYSTEM

For the past several years, the Hughes Torrance Research Center has successfully used the $AsCl_3/Ga/H_2$ VPE systems to grow undoped and doped GaAs epitaxial layers for ion implantation or FET device fabrication. The computer controlled VPE reactor and the reactor tube are shown in Figures 2-1 and 2-2, respectively. This reactor can grow as many as four wafers simultaneously. The key to successful growth of device quality GaAs materials lies in the ability to control background impurities, surface morphology, thickness and doping. These properties are strongly influenced by growth conditions such as temperature, substrate orientation, growth rate, and $AsCl_3/H_2$ ratio. The most commonly used n-type dopants in GaAs are S and Si which are often introduced by means of dilute H_2S/H_2 or SiH_4/H_2 gaseous mixtures. Sulfur doping is especially popular among the epi material suppliers since it can provide the widest range of doping density. We have developed the Si doping technique using a $SiCl_4/AsCl_3$ liquid solution. This technique has yielded an excellent GaAs epitaxial channel layer for FETs. Using this doping source does not require the metering of small gas streams as is required for other methods. In addition, the solution is stable and has a long shelf life since $SiCl_4$ and $AsCl_3$ are miscible over the entire composition range.

The $SiCl_4/AsCl_3$ liquid doping solution can be adjusted over a wide range of compositions in order to vary the chemical concentration of Si doping in GaAs epitaxy. Figure 2-3 shows the chemical concentration of Si as a function of the $SiCl_4$ mole fraction in the doping solution. The upper theoretical curve in Figure 2-3 is obtained from the assumption that silicon reaches an equilibrium condition without depleting GaCl and forming HCl at the surface of GaAs substrate due to growth of the GaAs film. On the other hand, the lower calculated curve takes into account these effects on the epitaxial growth. The experimental results should fall between the two curves. The unique ability offered by this silicon liquid doping method is the control of the carrier concentration over an extremely wide range from the low $10^{16}cm^{-3}$ to the mid $10^{19}cm^{-3}$. Therefore, this technique is suitable for growing an n-layer and n^+ contract layer sequentially by simply changing the mole fraction of $SiCl_4$. On the other hand, fine adjustment in the doping level can be achieved by adjusting both the H_2 flow rate and the temperature of the $SiCl_4/AsCl_3$ doping solution. Figure 2-4 shows the free carrier concentration as a function of

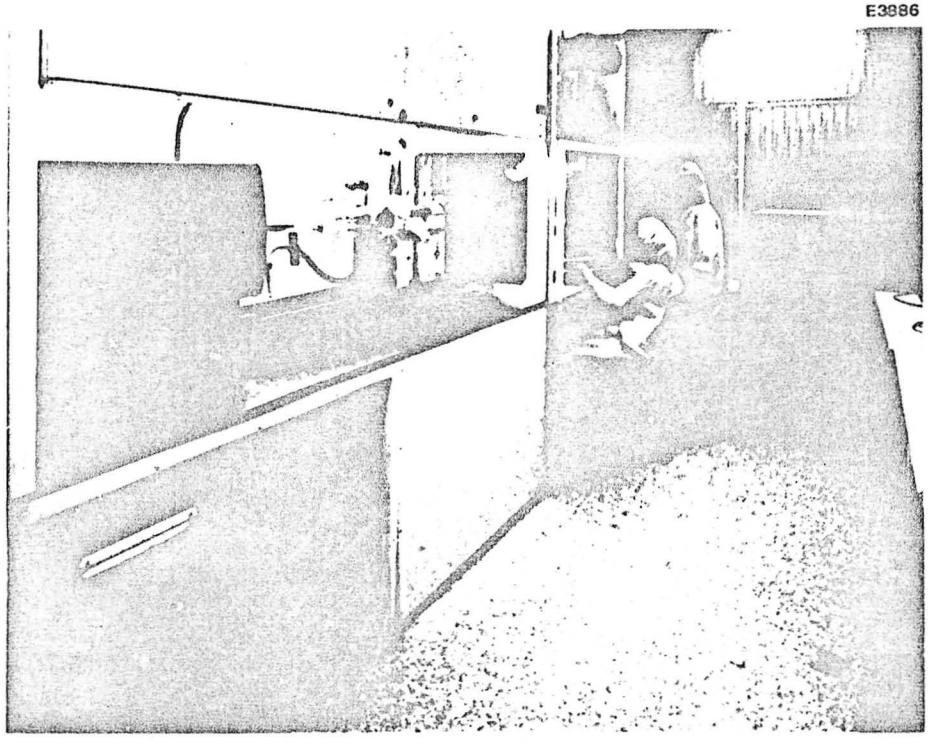


Figure 2-1 Computer controlled VPE reactor.

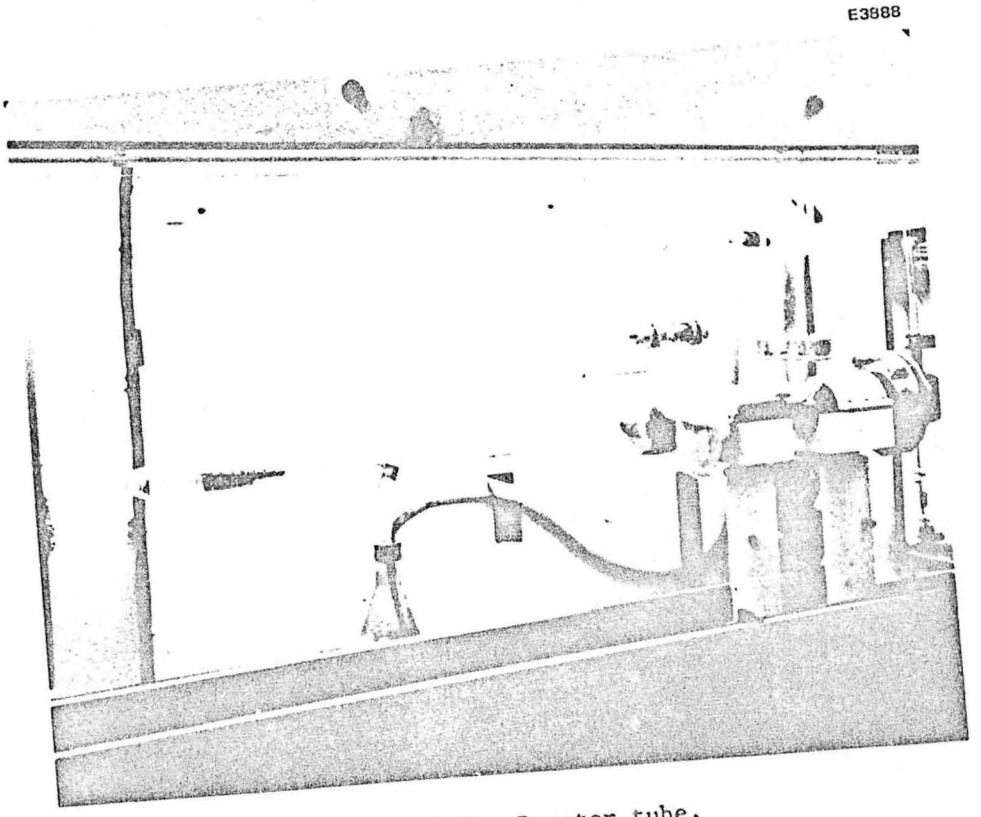


Figure 2-2 Reactor tube.

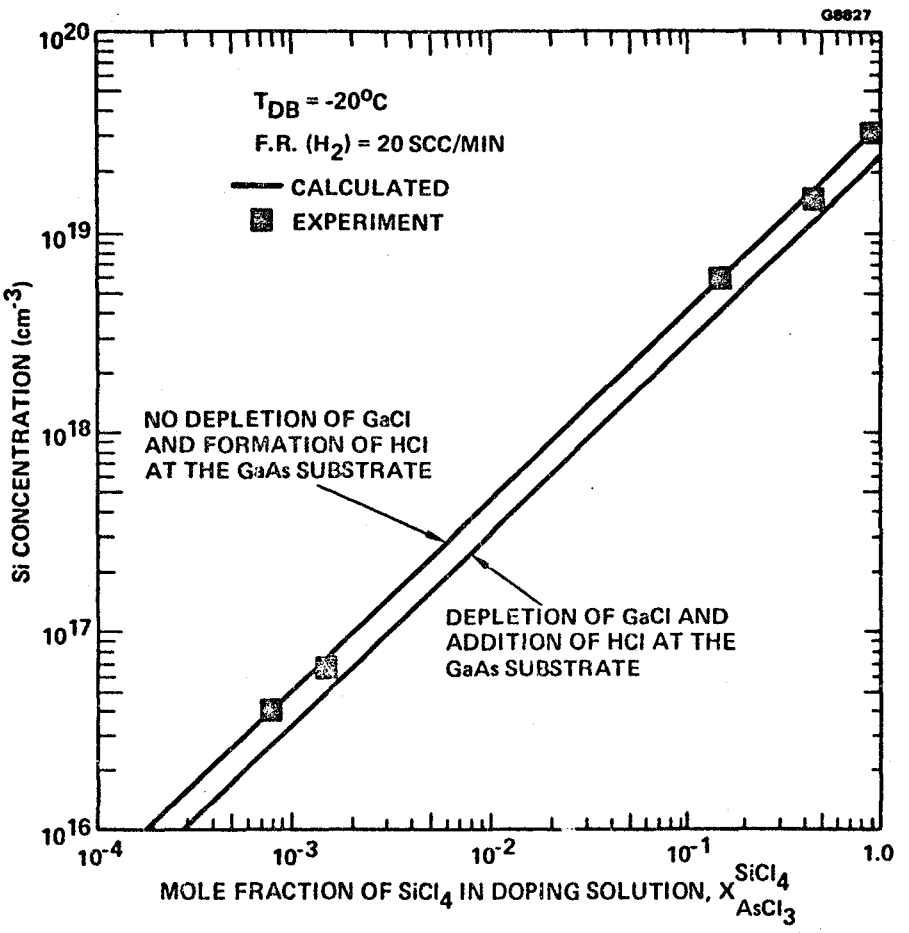


Figure 2-3 Si chemical concentration in a GaAs epitaxial layer as a function of mole fraction of $SiCl_4$ in the doping solution for a flow rate F.R. = 20 scc/min at a doping bubbler temperature T_{DB} = -20°C.

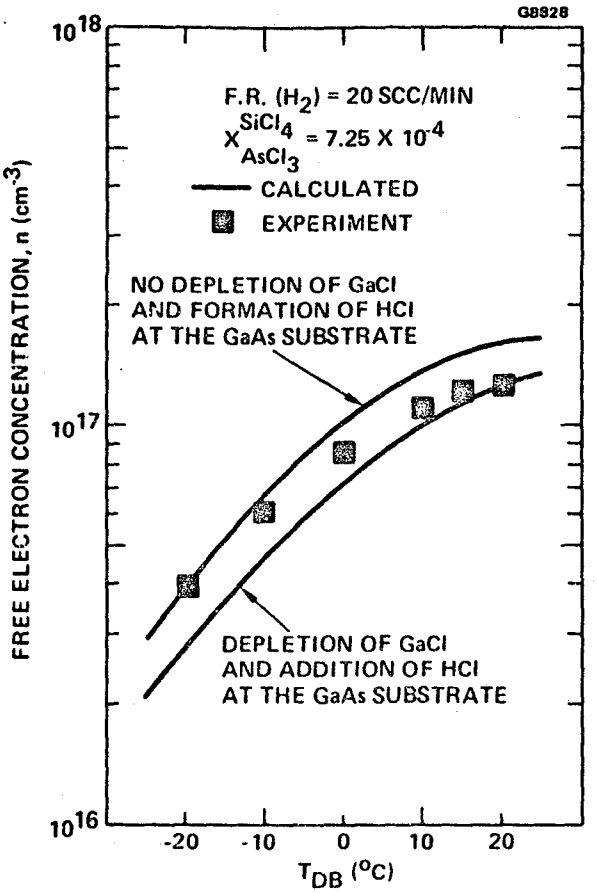


Figure 2-4 Free electron concentration from C-V measurements as a function of doping bubbler temperature for F.R. (H_2) = 20 scc/min and mole fraction of $SiCl_4$ in $AsCl_3$ = 7.25 x 10^{-4}.

the dopant solution temperature at a fixed H_2 flow rate. The variation of the doping bubbler temperature from $-20^{o}C$ to $+20^{o}C$ results in the concentration varying from $4x10^{16}$ to $1.3x10^{17}cm^{-3}$. Figure 2-5 shows the varied electron concentration from 1.0 to $1.9x10^{17}cm^{-3}$ obtained by changing the H_2 flow rate from 20 to 50 scc/min.

2.2 VPE REACTOR RESULTS

Figure 2-6 shows a concentration versus depth profile of a 0.22 μm thick Si doped layer grown on a 2 μm thick undoped compensated buffer layer. The electron concentration decreases from 10^{17} to $10^{16}cm^{-3}$ within 550 Å at the interface between the Si doped layer and the undoped buffer. The lower curve in Figure 2-6 shows the background impurity in the buffer layer. A chemical concentration profile obtained from SIMS for a thick Si doped layer illustrates doping uniformity in depth as shown in Figure 2-7. The flatness of the Si chemical profile in the active layer indicates that an excellent doping uniformity can be obtained using the $SiCl_4/AsCl_3$ liquid solution.

The measured room temperature Hall mobilities versus electron concentration are shown in Figure 2-8. In this figure, we also show Rode's[2] (1975) curve for a compensation ratio $(N_D + N_A)/n$ of unity. This curve was obtained based on both polar mode and ionized impurity scattering. Our experimental values agree fairly well with this curve except at higher concentrations. The liquid nitrogen mobilities, which are dominated by ionized impurity scattering, are plotted as a function of the free carrier concentration in Figure 2-9. The measured mobilities fall slightly below the "no compensation" mobility curves by Rode[2] (1975) and Stillman and Wolfe[3] (1976), and above the curve by Poth et al[4] (1978). The disagreement between Rode's curve and our experimental data at the high concentration ($>10^{18}cm^{-3}$) is mainly due to enhanced compensation. This compensation effect has been verified by Hall effect measurement of electron concentration and SIMS measurement of the Si chemical concentration. In the range of 1 to $3x10^{17}cm^{-3}$ doping, which is the main interest of this program, the grown epitaxial n-layers have excellent room temperature mobilities of 4400 to 5000 $cm^2/V\text{-}s$ and liquid nitrogen Hall mobilities of 5800 to 8600 $cm^2/V\text{-}s$.

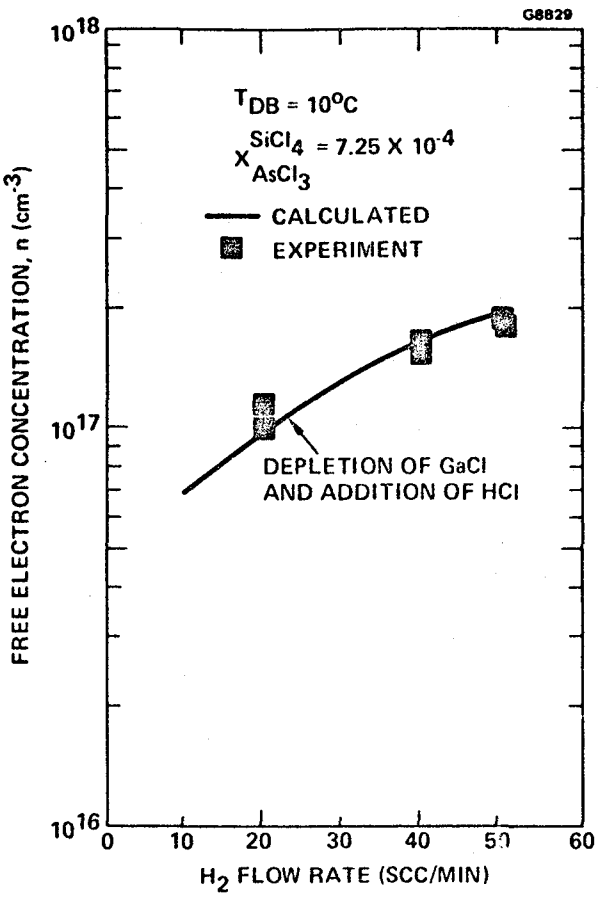


Figure 2-5 Free electron concentration from C-V measurement as a function of H_2 flow rate through the doping bubbler for T_{DB} = 10°C and mole fraction of $SiCl_4$ in $AsCl_3$ = 7.25 x 10^{-4}.

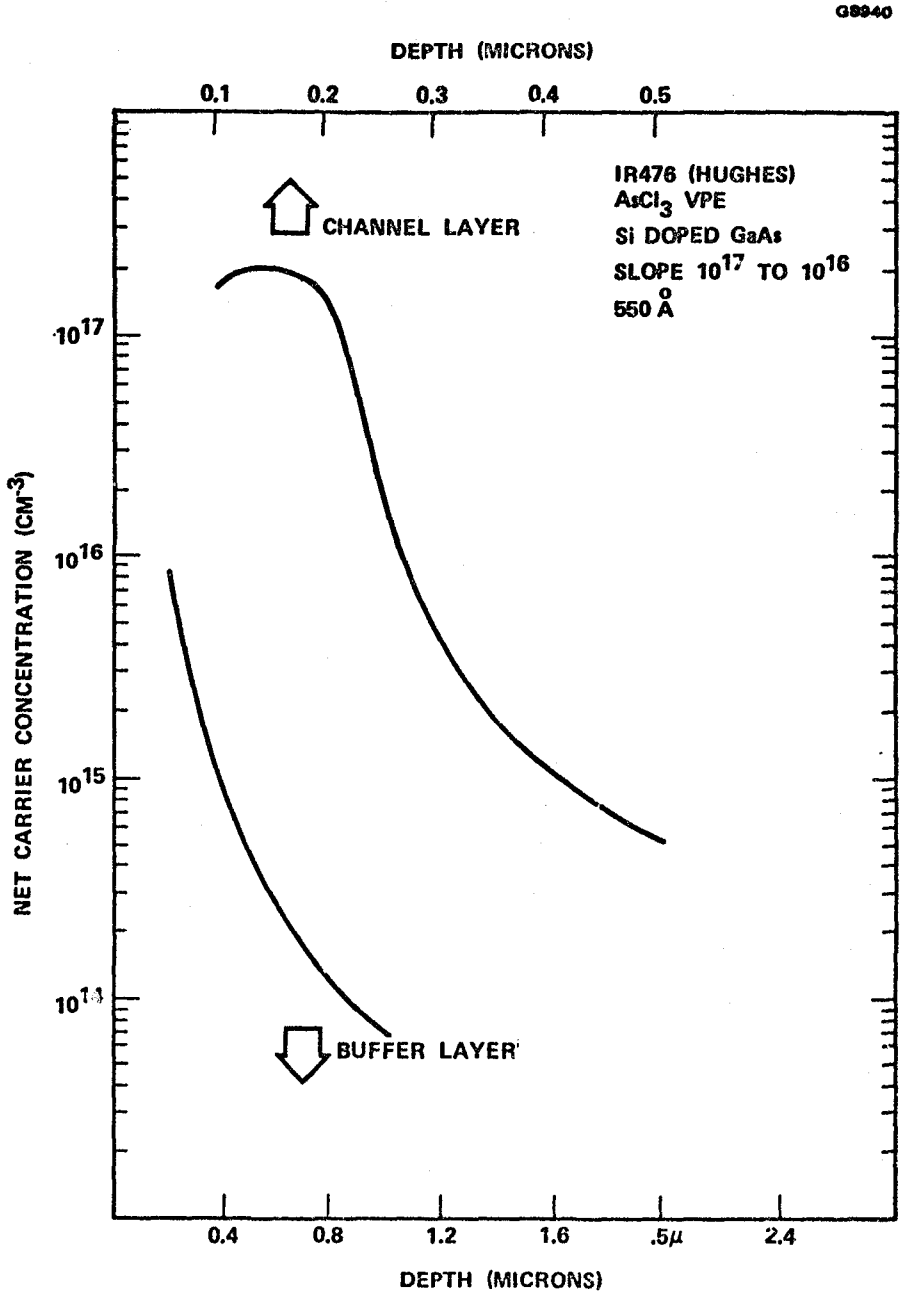


Figure 2-6 VPE profiles with the channel layer grown sequentially on an undoped buffer layer.

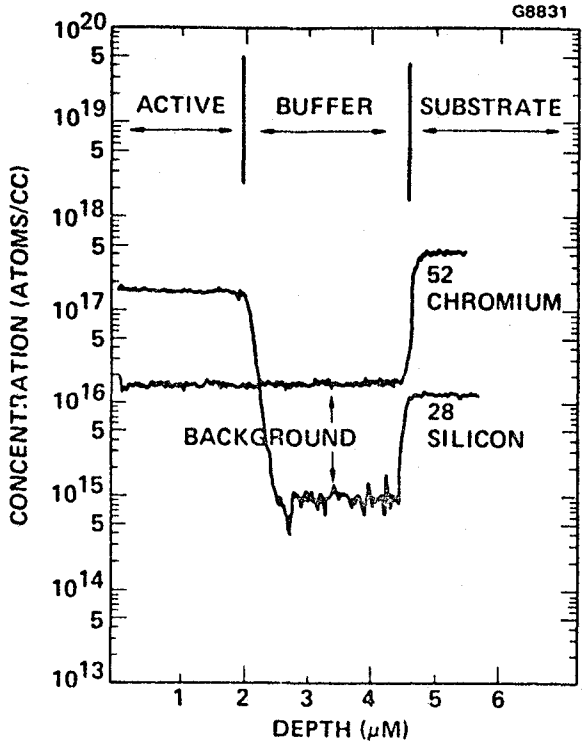


Figure 2-7 The Si and Cr SIMS chemical concentration profiles indicating uniformity of the Si-doped active layer over a 2 μm depth.

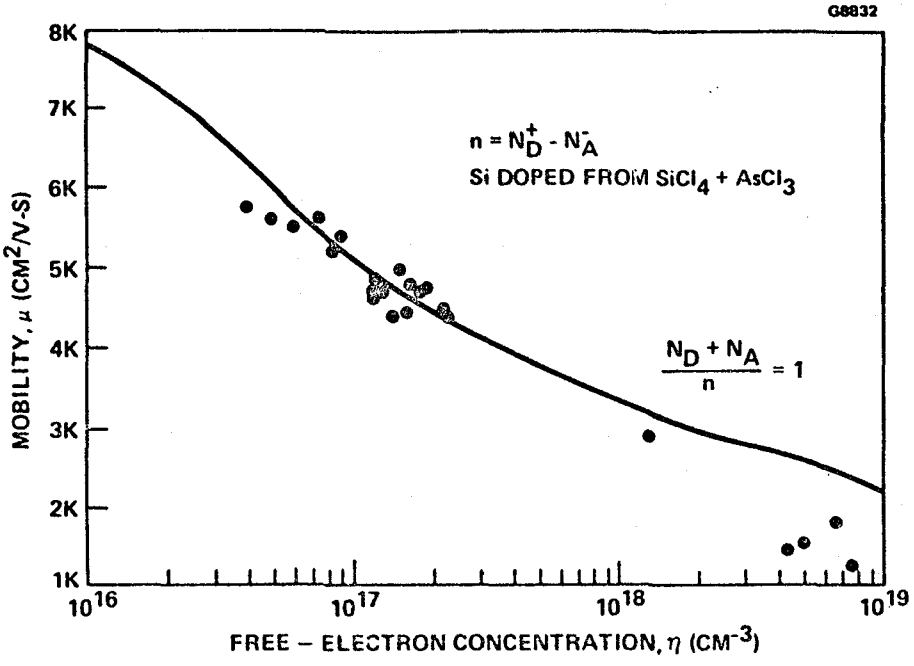


Figure 2-8 Room temperature mobility as a function of free electron concentration for the Si doped GaAs material with a calculated curve from Rode[2] (1975).

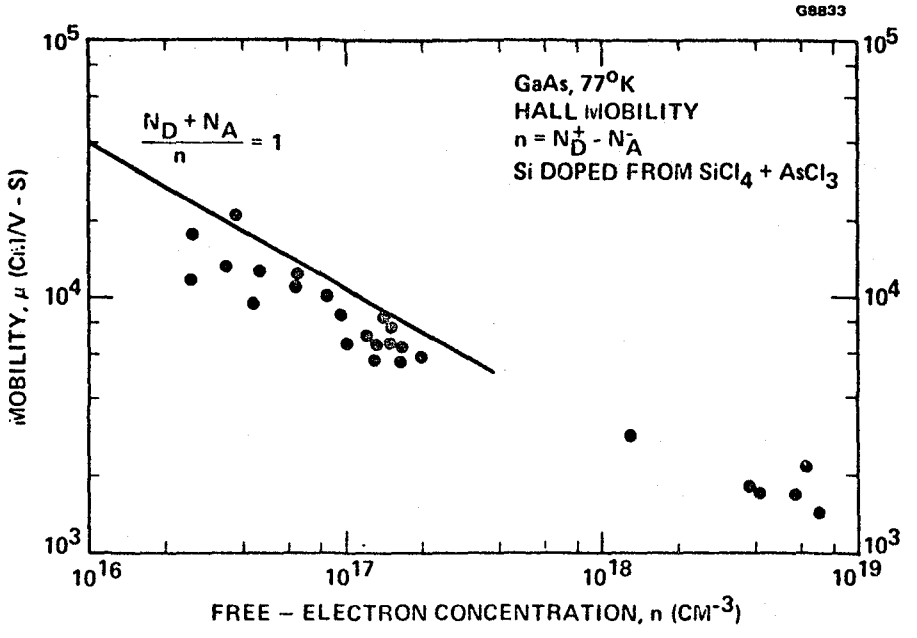


Figure 2-9 Liquid nitrogen mobility as a function of free electron concentration for the Si doped GaAs material with a calculated curve from Rode[2] (1975).

Since the completion of the VPE reactors, several hundred wafers have been processed. Some of the wafers were processed for buffer layers, some for low noise FET layers and some for power FET layers. The uniformity of carrier concentration, n, and thickness, d, has been evaluated by measurement of the nd product. An average variation of the nd product over a single wafer (8 cm^2 of area) is 6.7 percent. This figure is impressive, considering that the reactor is basically designed for multipurpose research use, with a fixed position of the wafer during the epitaxial layer growth.

The memory effect of Si doping in the reactor was a concern with pure undoped buffer layer growth since it might affect the quality of the buffer layer when the buffer and Si doped n type active layers were sequentially grown. To investigate this effect, we first grew a heavily doped layer with an Si level of $n_{Si} > 5x10^{18}cm^{-3}$. Then, the following run, an undoped layer with a thickness of 12 μm was grown. This undoped layer exhibited a 65,000 $cm^2/V-s$ liquid nitrogen mobility with a carrier concentration of $2x10^{15}cm^{-3}$. Photoconductivity was measured on this sample wafer at the University of Illinois (Prof. G.E. Stillman and coworkers) to determine the donor impurity in the buffer layer. Figure 2-10 shows the photo response as a function of wave number (cm^{-1}). The photo response data shown in Figure 2-11 illustrates that Si is the dominant species with Ge and S having slightly lower magnitudes. The photo response from the high purity undoped buffer layer is shown in Figure 2-12 as a reference in which S is the dominant donor impurity. The data indicates that considerable residual silicon is contained in the undoped buffer material and is responsible for the n-type conversion.

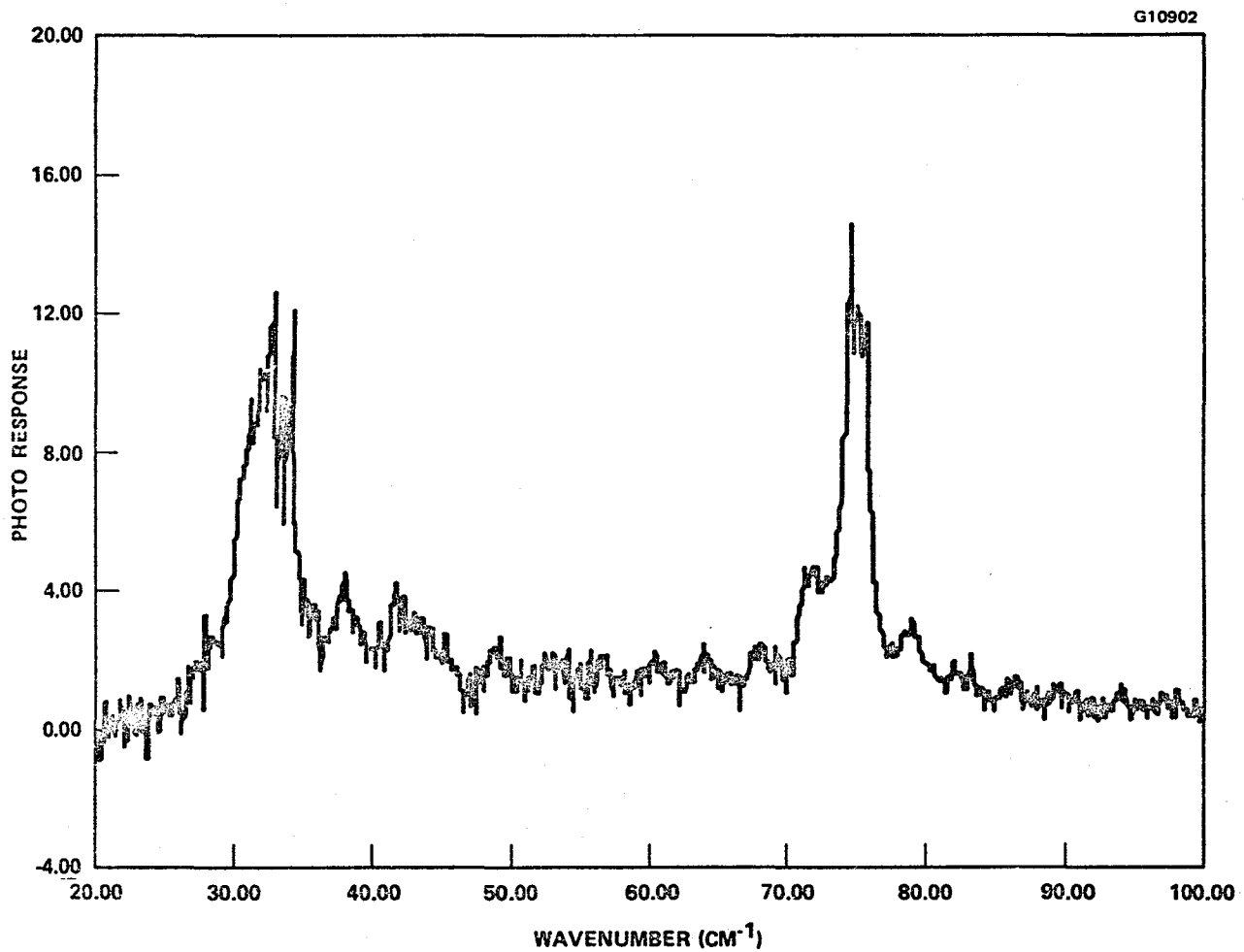


Figure 2-10 Photo response as a function of wavenumber.

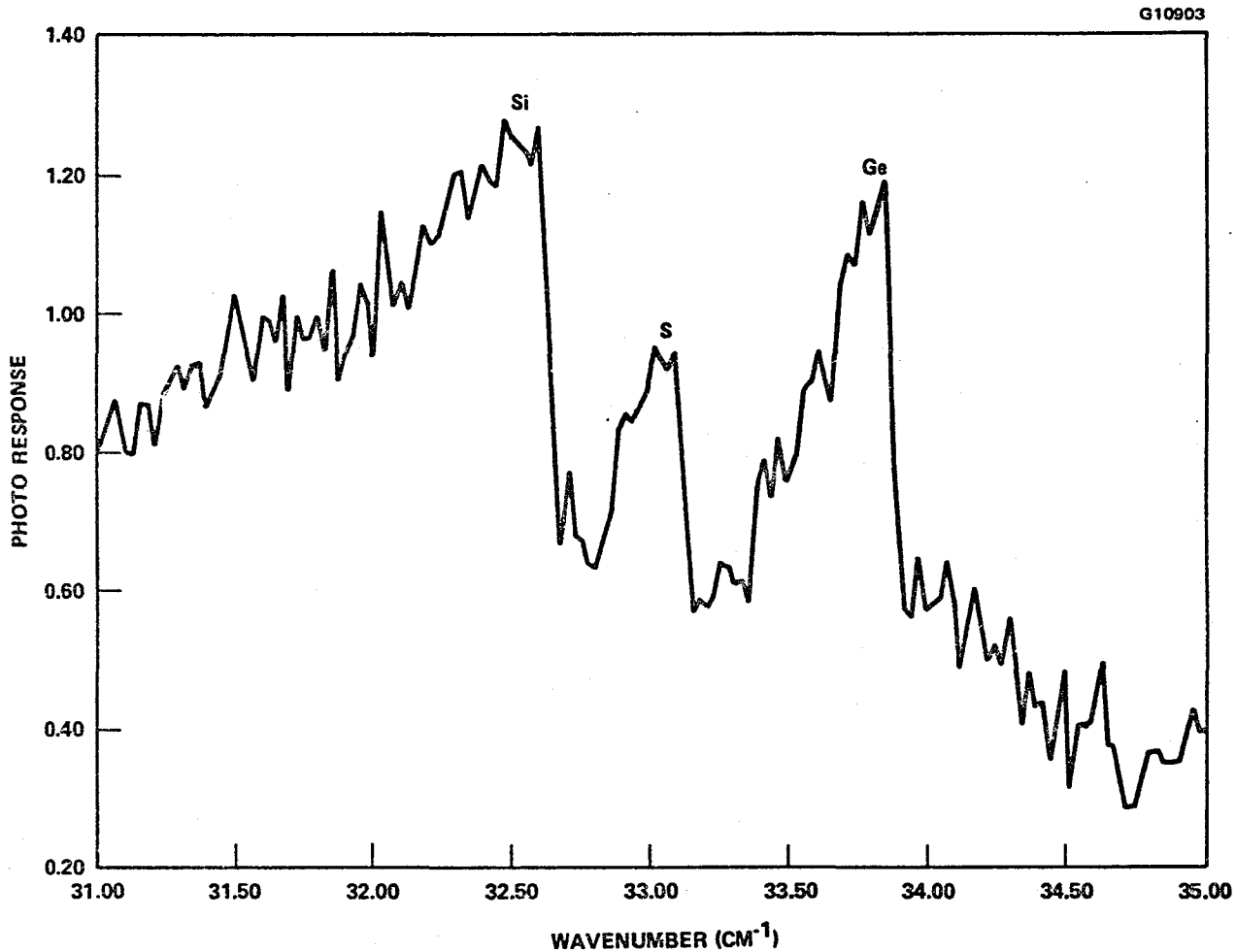


Figure 2-11 Photo responses of Si, S and Ge.

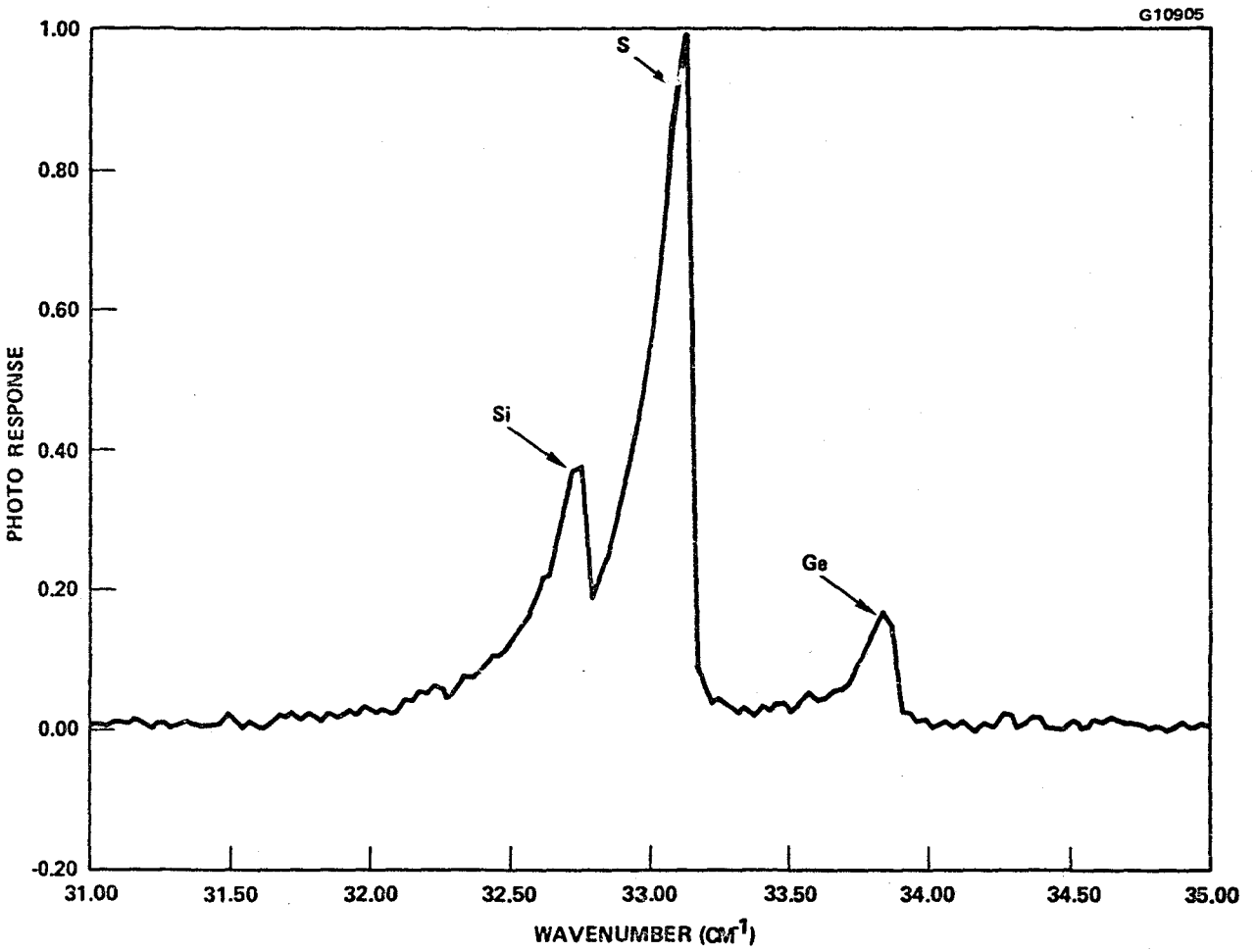


Figure 2-12 Photo response from the pure undoped buffer layer.

3.0 GaAs FET DEVICE DEVELOPMENT

Although extensive circuit design and device characterization effort was required, the single activity most responsible for the success of this program was the GaAs FET device development effort. This effort has resulted in new state-of-the-art performance levels for FET devices at 30 GHz. Three different device types were developed for this program:

1. A 30 GHz low noise device for the LNA.

2. A dual-gate FET device for use in the mixer.

3. A low phase noise FET device for use in the 25 GHz LO.

These key devices were developed at the Hughes Torrance Research Center as part of this program, and the results of the device development effort are described in the following sections.

3.1 LOW NOISE FET DEVICE DEVELOPMENT

During this program, three different types of low noise devices were employed. They consist of our standard PI300 device (0.5x300 μm E-beam defined gate), the E-FET device with all device patterns defined by the direct write E-beam technique, and the SM100 device series with a 0.25 μm gate. The PI300 device was originally designed for operation at X- and Ku-band frequencies with thousands of these devices being manufactured in the past several years. Since a vast amount of device characterization data is available from this device, it has been extensively used for this program's channel layer optimization. It was also used in the 25 GHz LO and in the LNA development early in the program.

The E-FET was developed as a transitional device from the PI300 device to the advanced 0.25 μm gate device. This experimental device was completely fabricated by the direct write E-beam technique without using photomasks so that the device dimensions or geometry can be frequently altered with a short turn-around time. This device with a 0.5 μm gate yielded the best noise figure performance at 30 GHz. This device provided the basis for the design of several types of the SM100 device series.

The SM100 series was designed and developed for the 0.25 μm gate FET. These devices established new state-of-the-art device performance levels for noise figure and gain at Ka-band frequencies. The results of a "spot check" of the reliability of a small sample of SM100 devices is presented in Appendix A.

3.1.1 Low Noise Device Design

A cross-sectional view of a low noise FET is shown in Figure 3-1. This FET has a channel configuration including a recessed gate but no n^+ contact layer. The noise figure of the FET can be estimated by using an equation derived by Hewitt et al.[5]

$$F_o(dB) = 10 \log_{10} \left\{ 1 + kfL \frac{5}{6} \left(\frac{N}{a}\right)^{1/6} \left[\frac{3.3\rho w^2}{hL} + 0.6w^2 \left(\frac{\rho f}{hL}\right)^{1/2} + \frac{1.8L_{sg}}{Na_2} + \left(\frac{0.18R_c}{Na_1}\right)^{1/2} \right]^{1/2} \right\} \quad (3\text{-}1)$$

where

L	=	gate length (μm)
L_{sg}	=	distance between source and gate edges (μm)
w	=	unit gate finger width (mm)
N	=	channel carrier concentration (10^{16} cm^{-3})
a	=	channel thickness under the gate (μm)
a_1	=	n-layer thickness under the source metallization (μm)
a_2	=	effective n-layer thickness (excluding surface depletion) between source and gate (μm)
h	=	effective gate metallization thickness (μm)
ρ	=	gate metal resistivity ($10^{-6}\Omega$-cm)
R_c	=	specific contact resistance ($10^{-6}\Omega$-cm^2)
k	=	constant related to material properties (0.034 is assumed)
f	=	frequency (GHz).

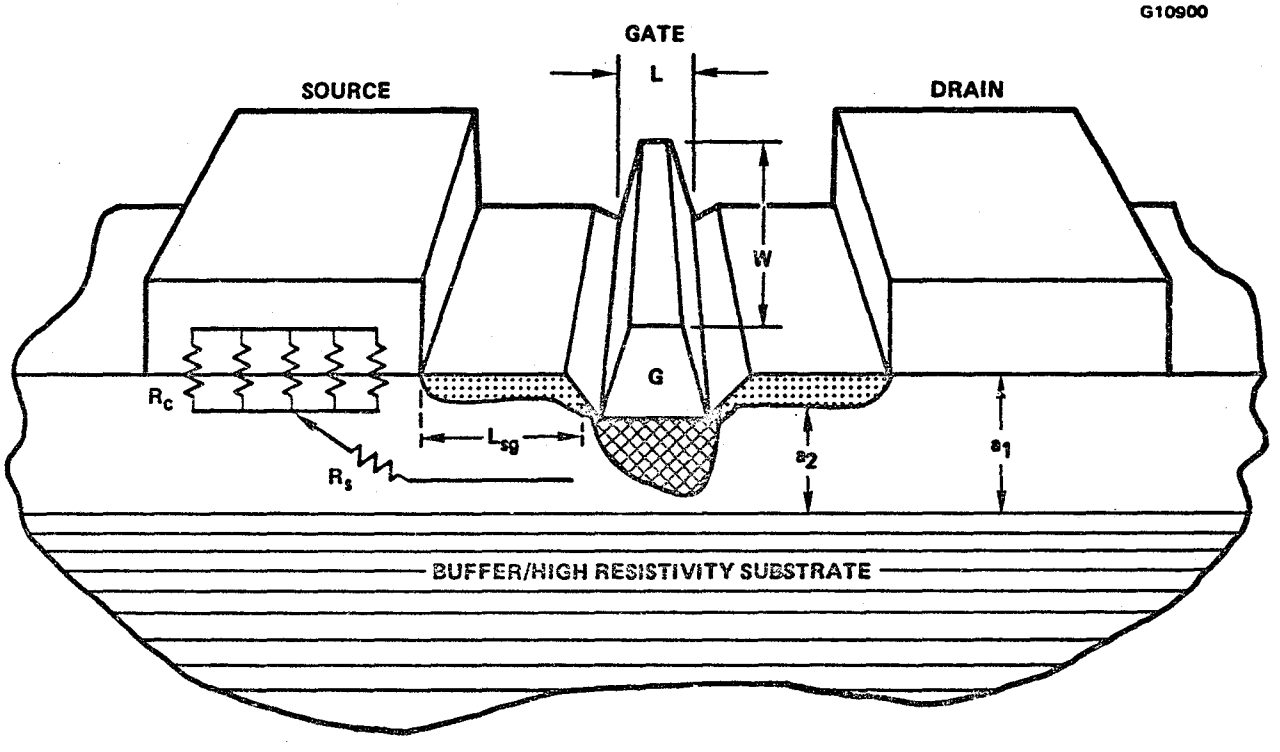


Figure 3-1 Cross-sectional view of recessed gate FET.

When the n^+ layer is added, the term $(1.8\ L_{sg})/(Na_2)$ in Eq. 3-1 can be split into two terms, one involving the n^+ layer and the other the n-layer which is effectively smaller. Hence, the equation shows that the noise figure should improve. In practice, the n^+ layer implementation requires a tighter control of the n-layer thickness which is difficult to achieve. Therefore, as our basic approach for the device material, we decided not to use the n^+ contact layer, although for comparison a few wafers with an n^+ contact layer were used. Instead, we placed the gate as close to the source electrode as possible to reduce the source resistance. By employing the E-beam direct write method for gate fabrication, we are able to consistently align the gate at a specified location within 0.5 μm of the edge of the source electrode. A deeply recessed structure for the gate and high doping density of the channel layer also contributed to reducing source resistance.

The device design parameters for our 0.5 μm gate and 0.25 μm gate FETs are tabulated in Table 3-1. The noise figures of the 0.5 μm gate and 0.25 μm gate FETs as a function of frequency, obtained by substituting the values in Table 3-1 into Eq. 3-1, are illustrated in Figure 3-2. The unit gate finger width of 75 μm and 38 μm was chosen for the 0.5 μm gate and 0.25 μm gate FETs, respectively. For comparison, Figure 3-2 includes the noise figure curve for the 0.25 μm gate FET with a unit gate finger width of 75 μm. In this case every parameter except gate length is the same as the 0.5 μm gate FET parameter. For comparison, the measured noise figures obtained from the various devices at different frequencies are also indicated in Figure 3-2. Several optimized PI300 (0.5x300 μm) devices were used to measure the noise figure at 12 GHz and 18 GHz. At higher frequencies, our newly developed 0.25 μm gate FET was primarily used for noise characterization. The measured noise figures from various 0.5 μm gate and 0.25 μm gate FETs follow the theoretically predicted curve quite well in the frequency range from 12 GHz to 30 GHz.

TABLE 3-1

DEVICE AND MATERIAL DESIGN PARAMETERS FOR THE
0.5 μm and 0.25 μm GATE DEVICES

Parameter	0.5 μm Gate	0.25 μm Gate (A)	0.25 μm Gate (B)
L (μm)	0.5	0.25	0.25
W (μm)	75.0	38.0	75.0
a (μm)	0.13	0.10	0.13
a_1 (μm)	0.36	0.32	0.36
a_2 (μm)	0.28	0.24	0.28
L_{sg} (μm)	0.5	0.5	0.5
h (μm)*	0.4	0.15	0.4
ρ ($10^{-6}\Omega$cm)	3.0	3.0	3.0
R_c ($10^{-6}\Omega cm^2$)	3.0	3.0	3.0
N (10^{17} cm^{-3})	2.5	2.5	2.5
K	0.034	0.034	0.034

*Effective height since the gate cross section is not a rectangle.

3.1.2 E-FET Development

As a part of our approach to optimizing the FET design for Ka-band applications, a basic geometry consisting of an array of four gate fingers was designed. Four versions of that geometry are illustrated in Figure 3-3. The device pattern was generated by a CAD pattern generator which operates in conjunction with our electron beam lithography system. All four mask layers of the device pattern -mesa, source and drain, gate, and overlay patterns - were directly defined by the E-beam microfabrication system. No photolithography was used to fabricate the device. This device is designated the E-FET.

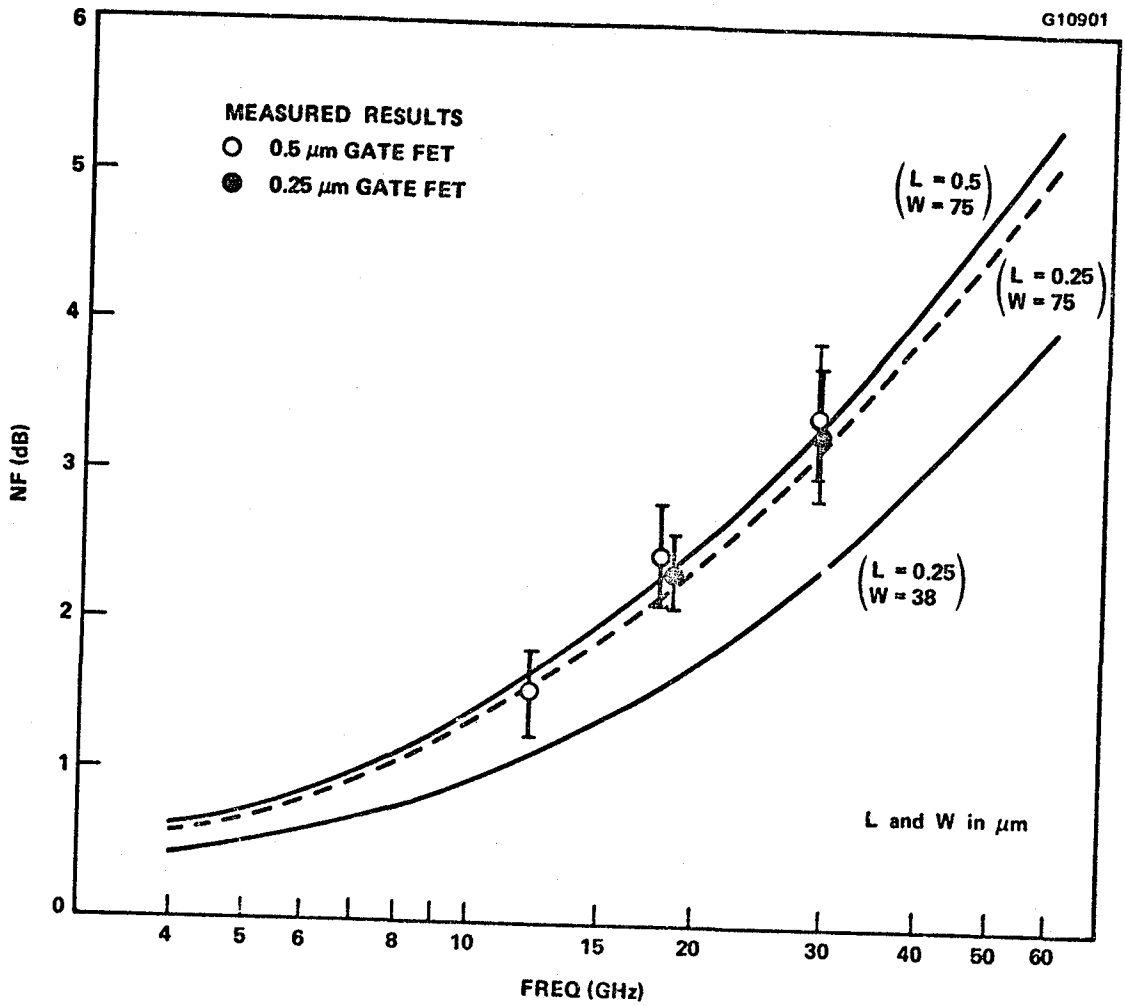


Figure 3-2 Calculated noise figure as a function of frequency for 0.25 μm and 0.5 μm gate FETs and measured results.

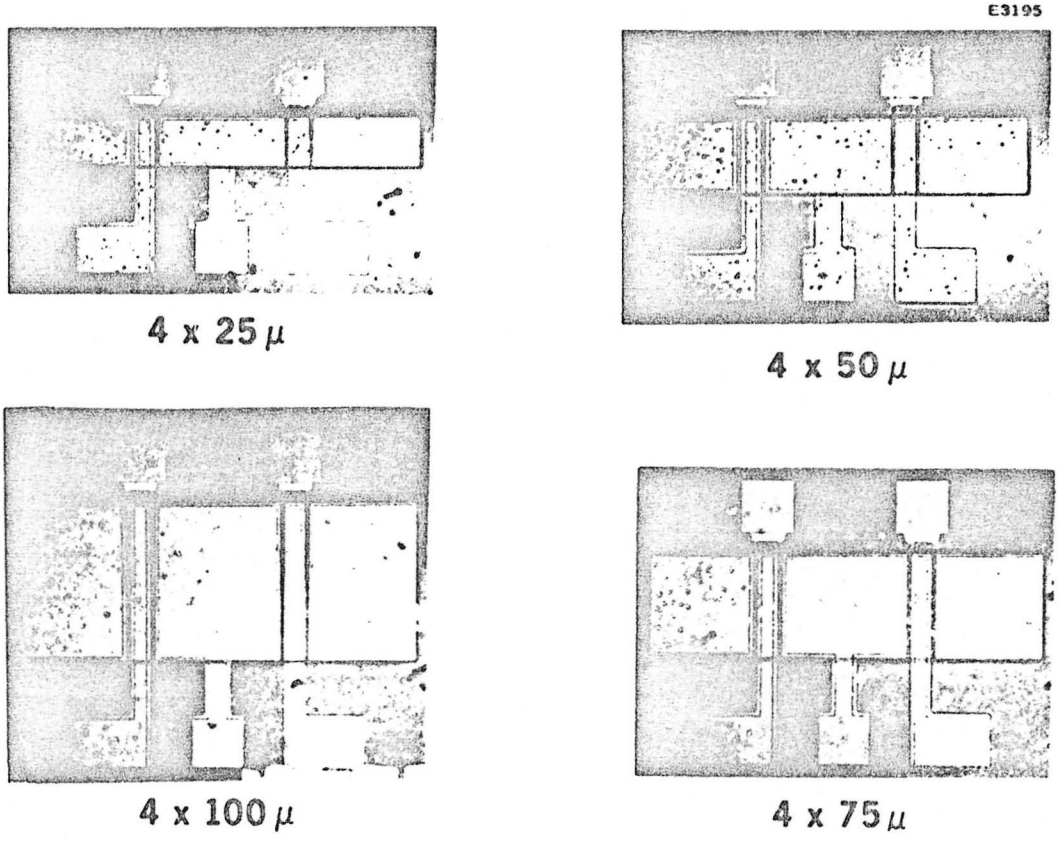


Figure 3-3 E-FETs with various finger widths.

Major device geometry parameters to be optimized are the gate length, gate width, the location of the gate in the channel with respect to the source, the depth of the gate recess, and the size of the gate and drain pads. This basic device pattern offers great flexibility for varying the gate finger width in the range of 25 to 100 μm and the gate length from 0.25 to 0.5 μm. For example, the devices shown in Figure 3-3 illustrate unit gate finger widths of 25 μm, 50 μm, 75 μm and 100 μm.

During the E-FET development, we employed various channel materials, namely, VPE, LPE and ion implantation into the semi-insulating substrates and LPE buffer layers. The VPE channel devices have consistently produced the best performance in terms of gain and noise figure at all frequencies between 12 and 30 GHz. Again, the devices fabricated with an LPE channel exhibited high gain at Ka-band frequencies.[6,7] For material characterization purposes, a device gate width of 150 μm was selected. This gate width selection was based on impedance matching considerations at Ka-band frequencies. Measured S-parameters of three 150 μm FETs made from (1) a VPE channel, Lot M401, (2) a LPE channel, Lot 1429, and (3) an ion implanted channel (directly into a Cr-doped substrate), Lot 178, are shown in Figures 3-4, 3-5 and 3-6, respectively. All measurements were made with an automatic network analyzer (ANA) over a frequency range of 2 to 18 GHz.

Based on the S-parameters obtained from these devices, the element values of the 14-element equivalent circuit model, shown in Figure 3-7, were obtained for each device, and are summarized in Table 3-2. The device from lot M401 has an excellent g_m and τ. However, its G_d is the largest of the three lots. The source resistance of Lot M401 is lower than the others which is attributed to the offset and the recessed gate structure. The gate offset is illustrated by the SEM photograph shown in Figure 3-8. This picture also shows the deeply recessed gate into the channel. All devices made with VPE channels are fabricated with a recessed gate; the depth of the recess is approximately 0.25 to 0.35 μm. This deep recess is evident in Figure 3-8 in which the top of the approximately 0.5 μm high gate is almost level with the surface of the channel. Based on the equivalent circuit element values, the devices from lots 178 and 1429 are similar except for their drain-to-gate feedback capacitance. The distinctive LPE channel properties of very low reverse feedthrough capacitance,

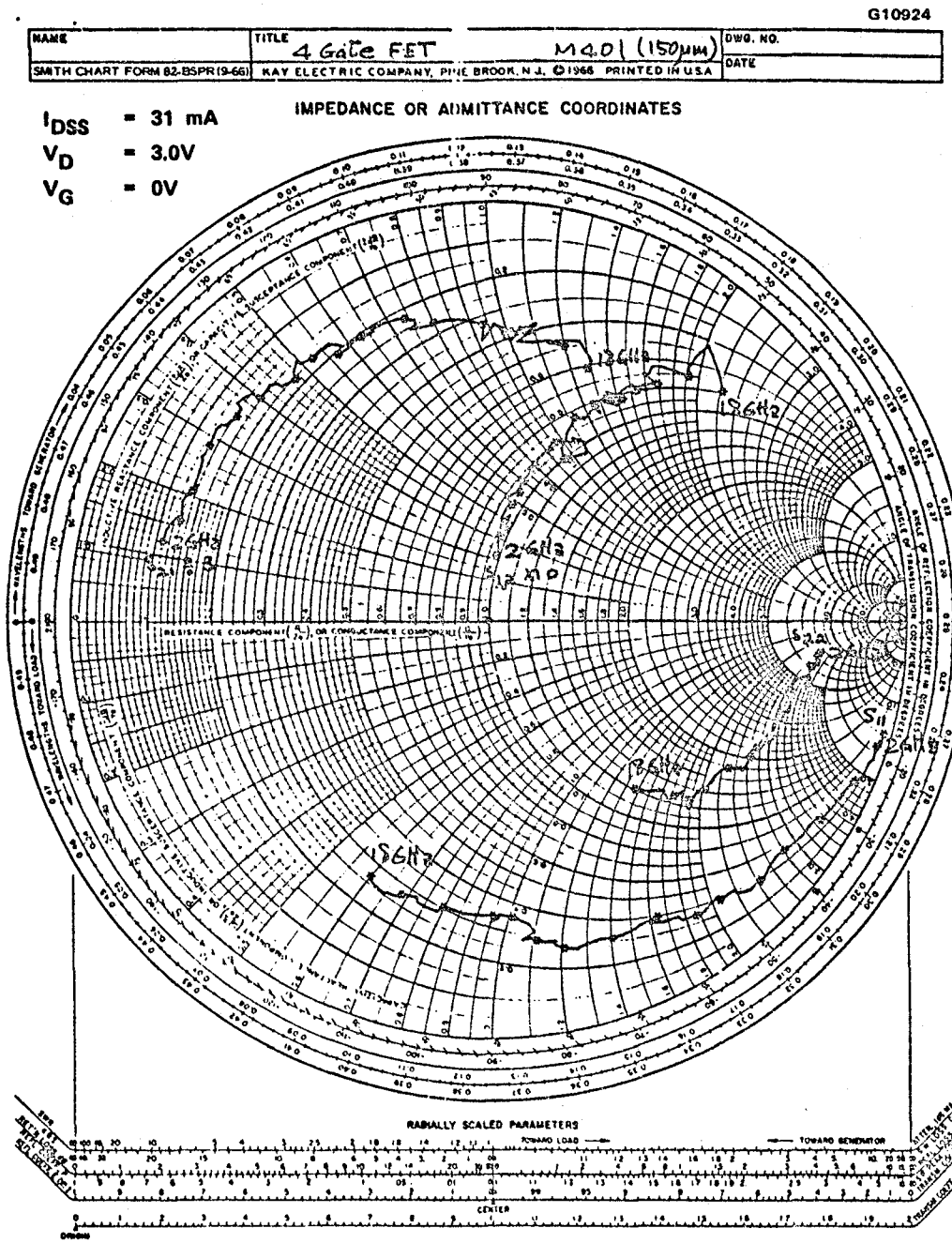


Figure 3-4 Measured S-parameters of FET lot M401 at I_{DSS} = 31 mA V_D = 3.0V and V_G = 0V. Each asterisk indicates a 1 GHz increment.

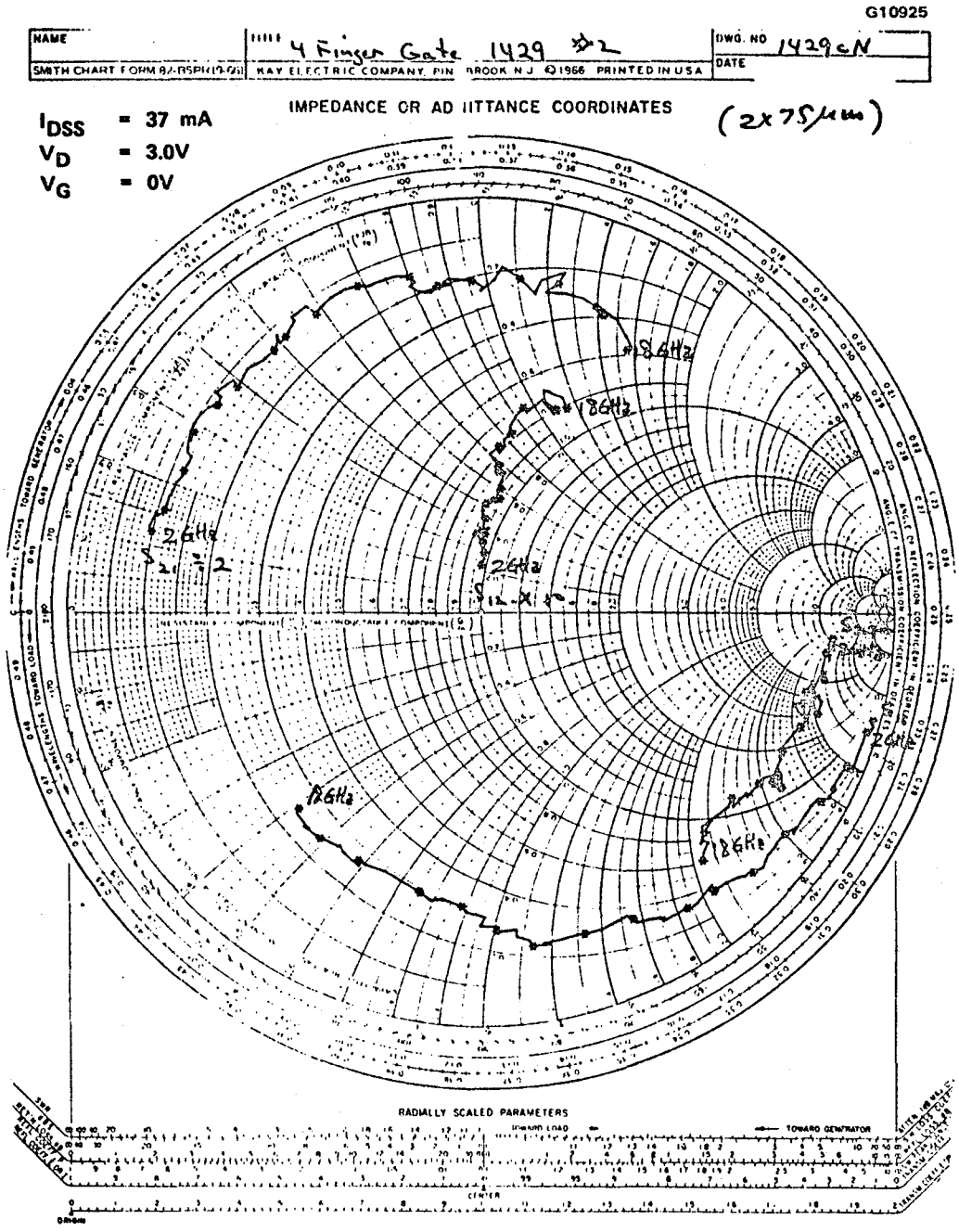


Figure 3-5 Measured S-parameters of FET lot 1429 at I_{DSS} = 37 mA V_D = 3.0V and V_G = 0V. Each asterisk indicates a 1 GHz increment.

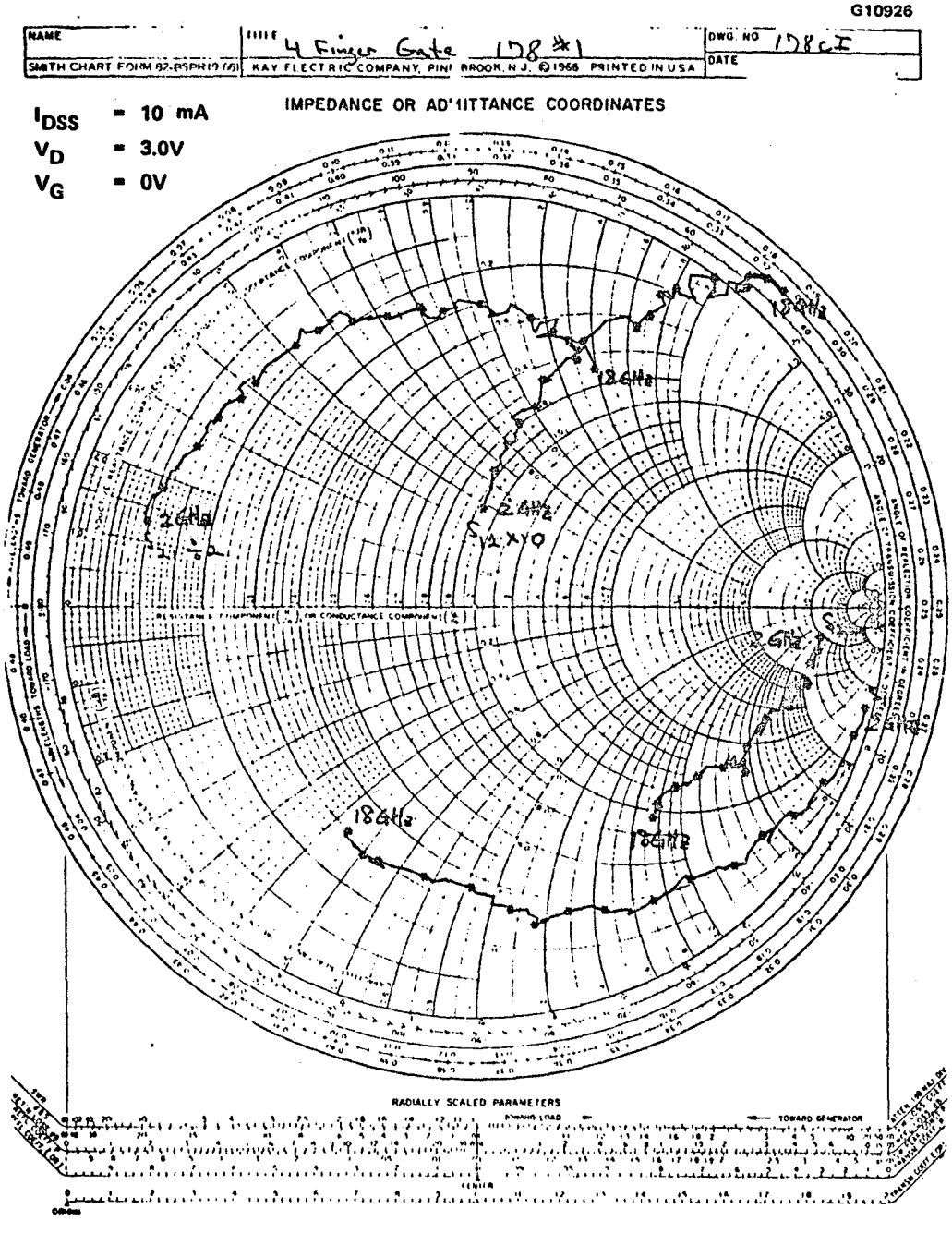


Figure 3-6 Measured S-parameters of FET lot 178 at I_{DSS} = 10 mA V_D = 3.0V and V_G = 0V. Each asterisk indicates a 1 GHz increment.

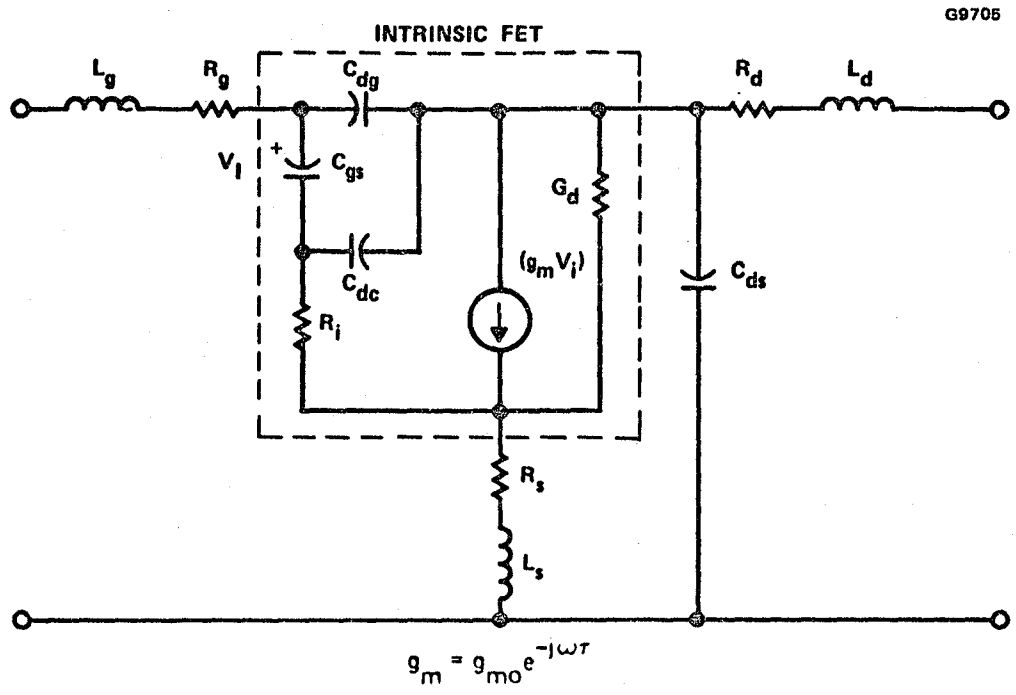


Figure 3-7 Equivalent circuit of a MESFET including all parasitics.

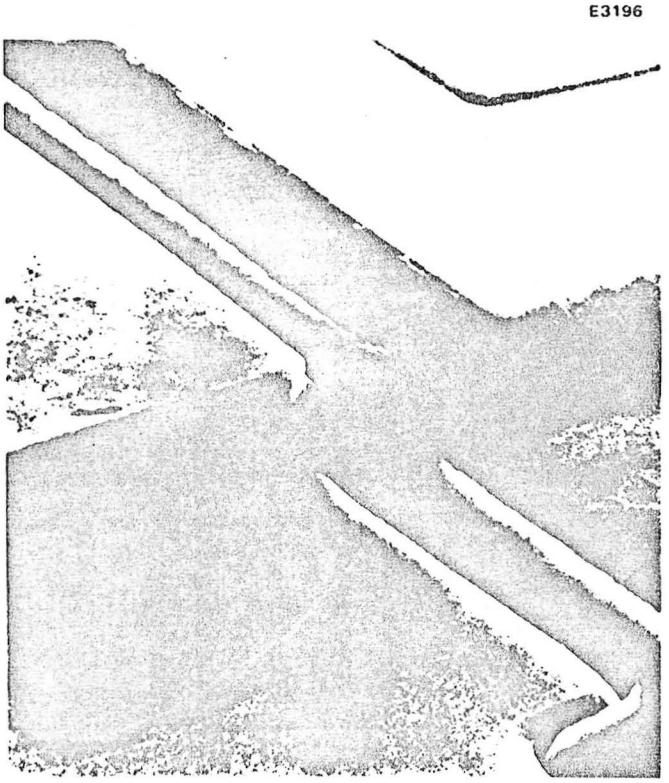


Figure 3-8 SEM of the E-FET with deeply recessed offset gate.

TABLE 3-2

EQUIVALENT CIRCUIT ELEMENT VALUES FOR
150 μm GATE WIDTH FETs

FET Lot #		M401	M401	1429	1429	178
Test Cond.	I_D (mA) V_D (V) V_G (V)	31 3 0	10 3 -0.9	37 3 0	10 3 -1.85	10 3 0
C_{gs} (pF)		0.163	0.105	0.161	0.112	0.163
C_{gd} (pF)		0.009	0.014	0.005	0.011	0.016
C_c (pF)		0.042	0.039	0.033	0.030	0.040
R_i (Ω)		2.34	2.91	1.60	2.14	3.23
g_m (m℧)		28.7	15.4	19.1	12.5	18.8
τ(psec)		1.98	2.11	3.15	2.67	2.67
G_d (ms)		2.54	2.42	1.90	2.06	1.94
L_g (nH)		0.147	0.160	0.268	0.268	0.155
R_g (Ω)		6.77	4.91	3.033	4.45	5.63
L_s (nH)		0.058	0.065	0.075	0.081	0.083
R_s (Ω)		2.26	2.85	2.98	4.01	3.35
L_d (nH)		0.368	0.352	0.164	0.255	0.268
R_d (Ω)		2.38	1.83	1.93	2.20	2.05
C_d (pF)		0.011	0.013	0.024	0.023	0.007

C_{dg}, along with low output conductance enhanced the high frequency response of this device. VPE and ion implanted devices consistently outperformed the LPE device at lower frequencies in terms of noise figure and gain; however, the LPE device insertion gain remained relatively constant over a broad frequency range.

The noise figure and gain of the E-FET LPE device (0.5x150μm gate) from lot 1429 at 29 GHz is illustrated in Figure 3-9. For comparison, the equivalent performance of the VPE device (0.5x150μm gate), lot 401, is shown in Figure 3-10. A different device from lot 401 yielded a noise figure of 2.3 dB with an associated gain of 8.1 dB at 18 GHz. This is the best combined noise figure and associated gain performance (2.6 dB noise measure) from the E-FET device series. The measured insertion gain $|S_{21}|$ of devices from the different lots, M401, 1429 and 178, are illustrated as a function of frequency in Figure 3-11. The ripples on the curves represent ANA system error and have no bearing on device characteristics. This figure clearly shows that the VPE device provides the highest insertion gain, while the LPE device exhibits a very flat insertion gain curve from 2 to 18 GHz.

3.1.3 SM100 Series Devices

Based on the device and materials information obtained from the E-FET device optimization, we designed a new mask set which contains several different device configurations, including a single stage 30 GHz monolithic low noise amplifier and several test patterns, in a 4x4 matrix form as shown in Figure 3-12. A detailed description of the individual devices which constitute the SM100 series "FET kit" is tabulated in Table 3-3. For the fabrication of SM100 series devices, we employed photolithography for every pattern generation except gate definition. Since the E-beam direct write method is employed for gate pattern generation, a gate length of either 0.25 μm or 0.5 μm can be selected. The gate width obtained from these SM100 series devices varies from 75 μm to 300 μm. Several different device geometries are included to investigate the effects of geometry on RF performance.

In the SM100 series device development task, a 0.5 μm gate was implemented for the first two runs in preparation for the 0.25 μm gate device fabrication. Noise figure and gain of the devices from these two lots, SM01 and SM02, are summarized in Tables 3-4 and 3-5. The noise figure results at 12 and 18 GHz

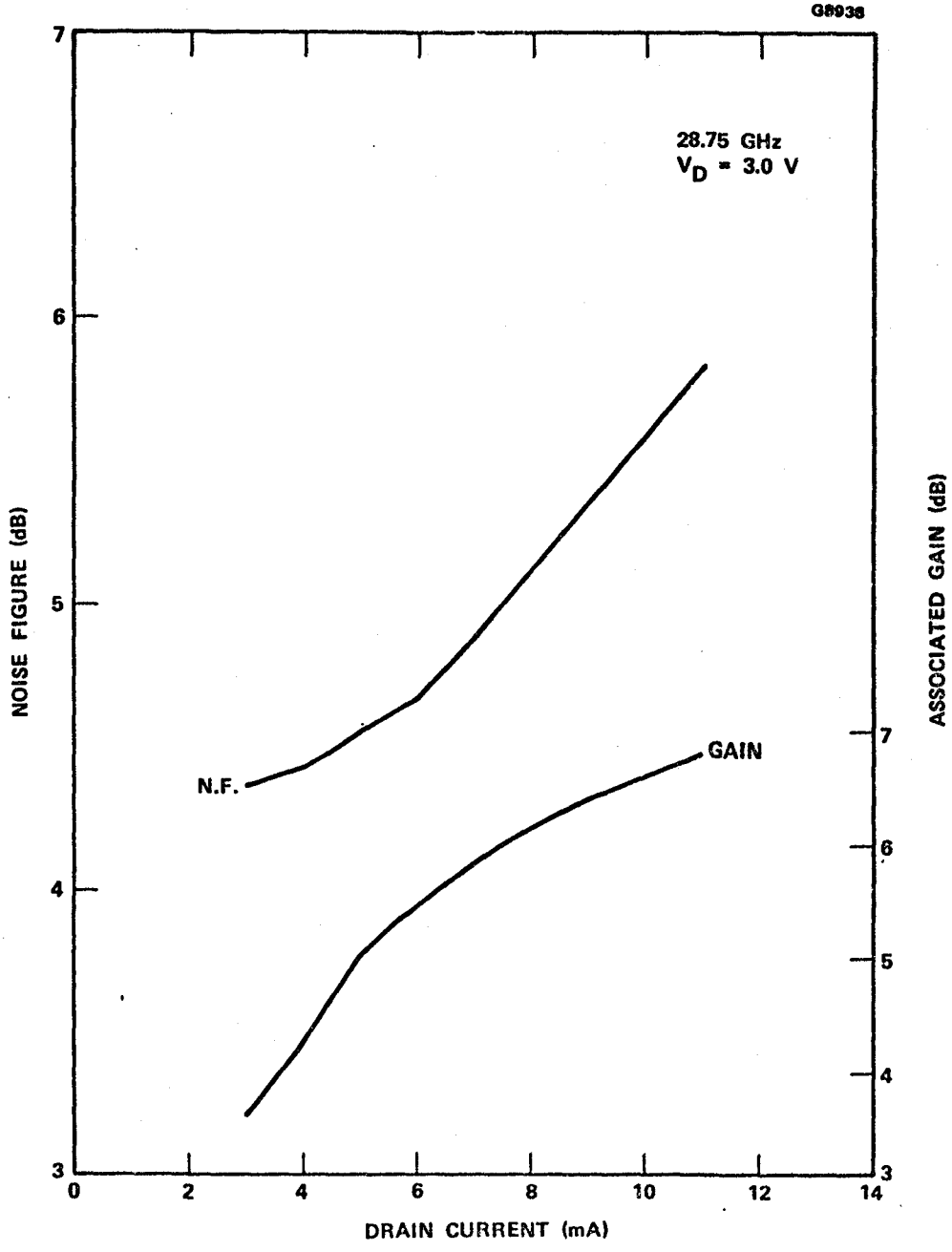


Figure 3-9 Noise figure and associated gain vs drain current for the LPE lot 1429 device.

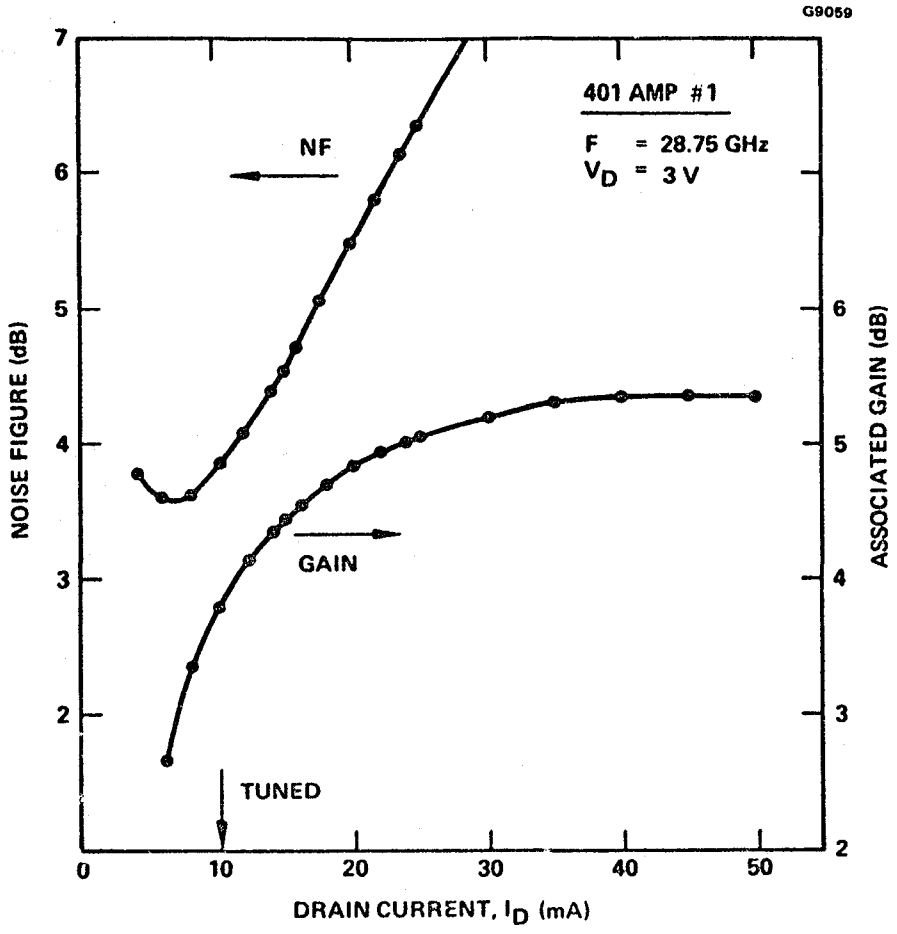


Figure 3-10 Noise figure and associated gain versus drain current for the VPE lot 401 device.

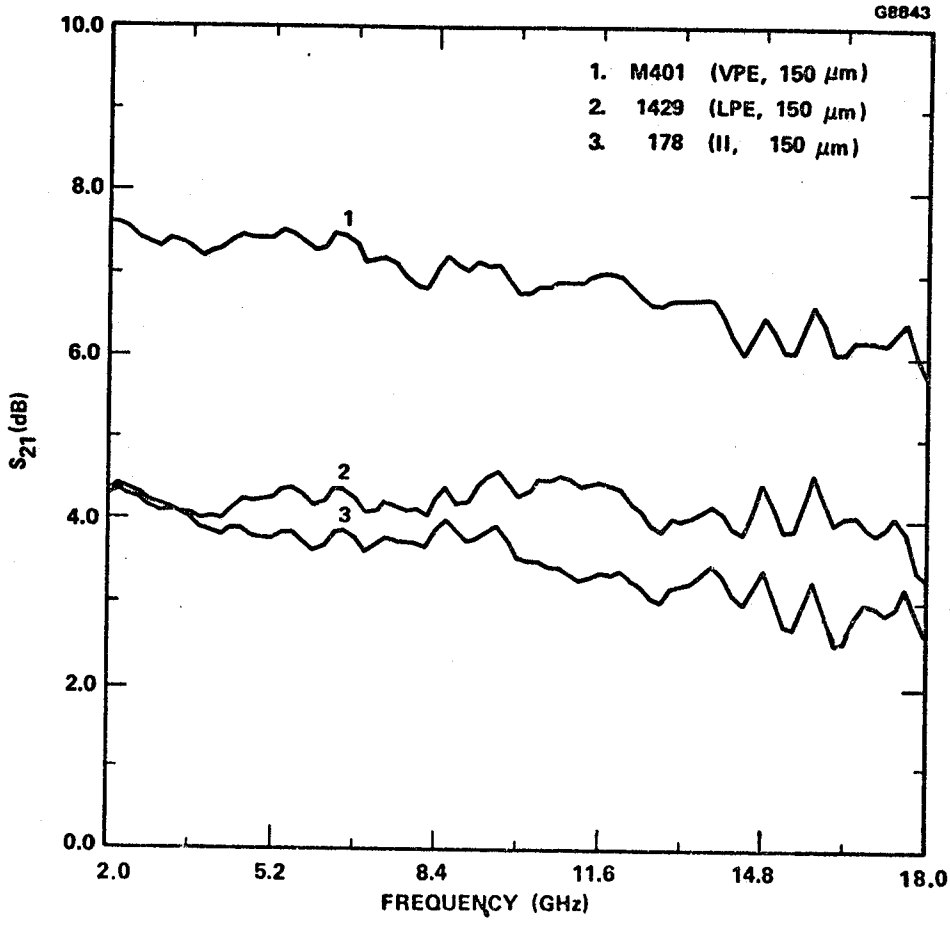


Figure 3-11 Measured insertion gain $|S_{21}|$ of 3 different FETs from 2 to 18 GHz.

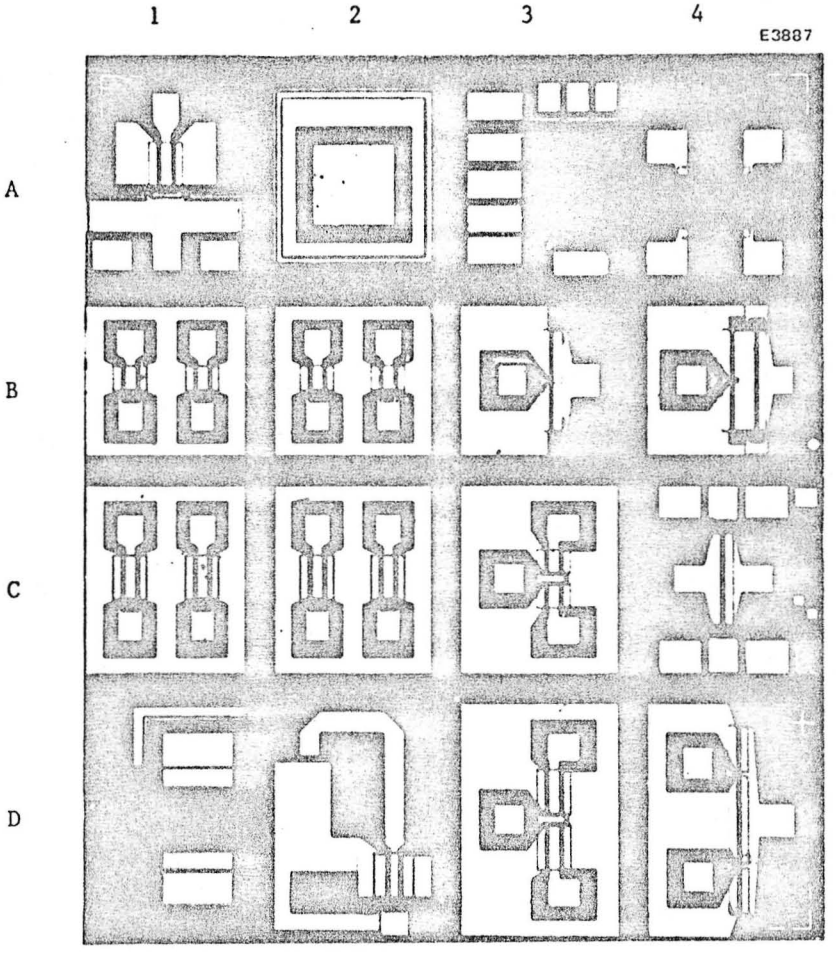


Figure 3-12 SM100 series devices.

TABLE 3-3

DESCRIPTION OF THE SM100 DEVICE MATRIX SHOWN IN FIGURE 3-12

Row	Col	Device and Test Patterns
A	1	On-Chip matched input 150 μm FET
A	2	Test pattern for CV measurement
A	3	Test pattern for ohmic contact and gate resistance
A	4	Test pattern for Hall mobility measurement
B	1	75 μm dual-cell FET with 3 μm channel length
B	2	75 μm dual-cell FET with 2.5 μm channel length
B	3	150 μm FET
B	4	150 μm cascode FET
C	1	150 μm dual-cell FET with 3 μm channel length
C	2	150 μm dual-cell FET with 2.5 μm channel length
C	3	150 μm FET
C	4	150 μm common gate FET
D	1	Fat FET
D	2	30 GHz monolithic amplifier
D	3	300 μm FET
D	4	300 μm FET

TABLE 3-4

NOISE PERFORMANCE OF SM01 DEVICES

Device	Size (μm)	Minimum Noise Figure (dB)	Associated Gain (dB)	Maximum Available Gain (dB)	Frequency (GHz)
1	0.5x300	3.41	8.01	-	12.0
2	0.5x150	3.99	7.2	-	18.0
3*	0.5x150	5.1	5.1	7.3	28.75

*Amplifier level data

TABLE 3-5

NOISE PERFORMANCE OF SM02 DEVICES

Device	Size (μm)	Minimum Noise Figure (dB)	Associated Gain (dB)	Maximum Available Gain (dB)	Frequency (GHz)
1	0.5x150	2.72	10.6	13.98	12.0
2	0.5x300	1.91	10.34	13.24	12.0
2	0.5x300	2.44	8.9	-	14.0
1	0.5x150	3.56	6.9	9.8	18.0
2	0.5x300	3.5	5.9	8.4	18.0
3	0.5x75	4.07	6.97	9.48	18.0
4*	0.5x150	4.6	6.0	-	28.75

*Amplifier level data

are not particularly good compared with some of our 0.5 μm gate E-FETs and PI300 FETs. For lots SM01 and SM02 we placed the 0.5 μm gate in the middle of the 2.5 μm source-drain spacing instead of offsetting the gate toward the source electrode. This produced high source resistance which degraded RF performance. At 29 GHz, a noise figure of 4.6 dB with an associated gain of 5.5 dB was obtained from a SM02 device, B1.

Our first successful 0.25 μm gate lot was SM08. Due to the gate opening which was reduced by a factor of two from the 0.5 μm gate structure and to anisotropic chemical etching characteristics, we experienced some initial difficulty in fabricating the 0.25 μm gate with a deeply recessed structure. By implementing either the double recessed configuration or a thinner channel layer, this problem was alleviated somewhat but not completely. A SEM picture of the smallest SM100 series device, B1, and a magnified view of the channel topology are shown in Figure 3-13(a)and (b), respectively. The gate length of this device is 0.25 μm. As seen in the figure, the gate of this particular device is placed in the middle of the channel with a relatively shallow recess structure.

Tables 3-6 and 3-7 summarize the device performance at 12 GHz and 18 GHz obtained from various device geometries from two lots, SM08 and SM10. In general, these devices yielded good combined performance of noise figure and gain at these two frequencies. While the 0.5 μm gate FETs demonstrated better noise performance at these frequencies, these 0.25 μm gate devices produced significantly higher gain over a wide range of bias conditions. Figure 3-14 supports this observation by showing the measured insertion gain $|S_{21}|$ of a 0.25x150 μm gate FET from Lot SM10 as a function of frequency from 2 to 18 GHz. The value of $|S_{21}|$ at 18 GHz is a high value of 7.5 dB.

With the limited number of lots, the device geometry effect on RF performance did not clearly emerge. However, the device geometry identified as C3, consisting of one gate feed and two separate drain feeds with four 38 μm gate fingers, demonstrated exceptionally high device gain. This geometry also exhibited a higher $|S_{12}|$ value compared to other device types. For comparison, the measured S-parameters of several different types of 0.25x150 μm gate devices are shown in Figures 3-15, 3-16 and 3-17. The device C2 consists of

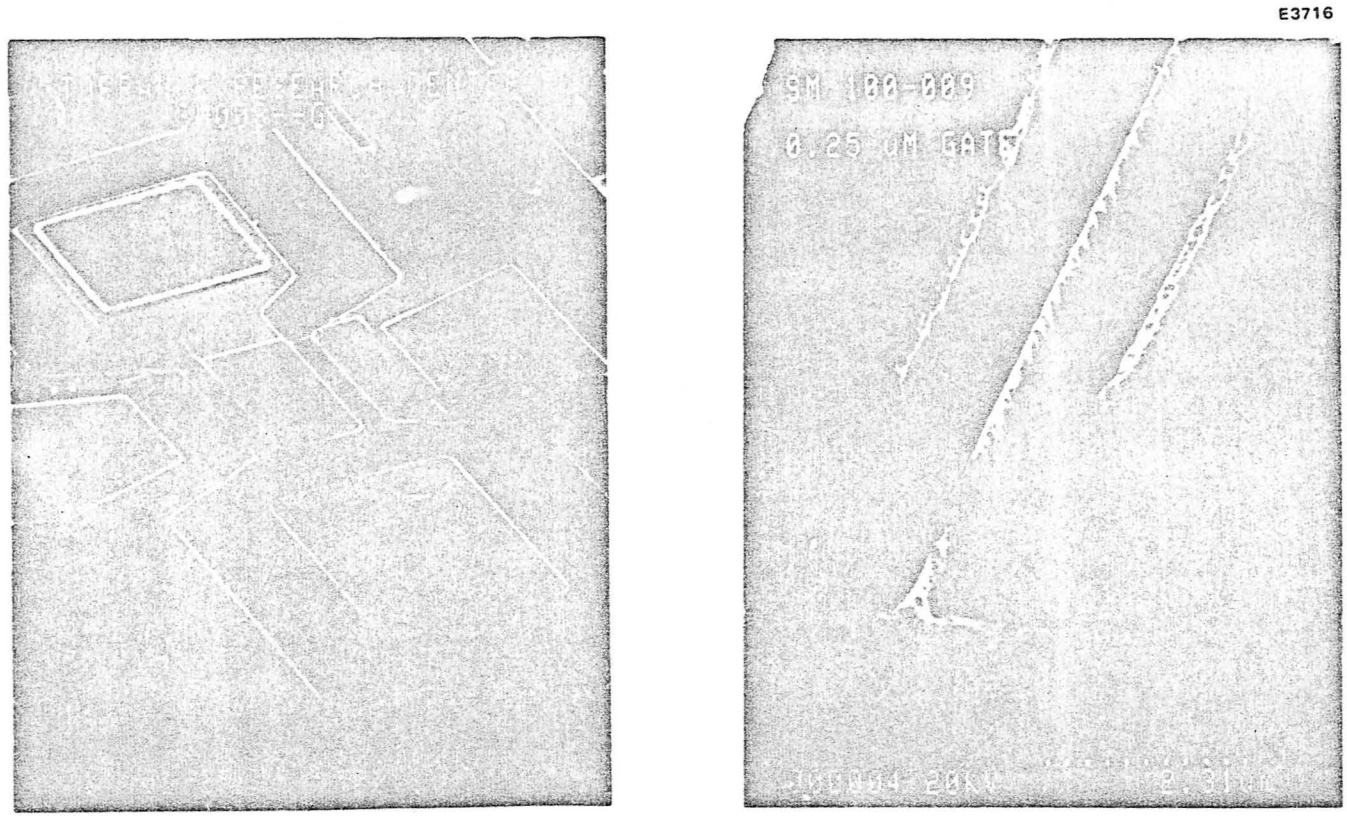


Figure 3-13 SEM photograph of 0.25x75 μm MESFET and magnified view of 0.25 μm gate.

TABLE 3-6

NOISE AND GAIN PERFORMANCE OF SM08 0.25 μm GATE FETs

Device ID	Device Type (Fig. 3-12)	Device Gate Width (μm)	Minimum Noise Figure (dB)	Associated Gain (dB)	Maximum Available Gain (dB)	Test Frequency (GHz)
1	D3	300	1.82	10.58	13.62	12.0
2	D4	300	2.59	9.82	11.44	12.0
3	B3	150	2.94	9.96	-	12.0
4	C3	150	2.23	13.07	-	12.0
5	C3	150	2.47	9.07	12.57	12.0
6	B3	150	2.04	9.23	11.43	12.0
7	C2	150	2.49	12.1	14.87	12.0
1	D3	300	2.49	9.15	9.81	18.0
4	C3	150	2.97	7.36	-	18.0
6	B3	150	2.70	7.58	9.66	18.0
7	C2	150	3.15	8.45	11.13	18.0
8	B2	75	4.14	8.96	11.09	18.0

TABLE 3-7

NOISE AND GAIN PERFORMANCE OF SM10
0.25 μm GATE FETs

Device ID	Device Type (Fig. 3-12)	Device Gate Width (μm)	Minimum Noise Figure (dB)	Associated Gain (dB)	Maximum Available Gain (dB)	Test Frequency (GHz)
1	D3	300	2.34	10.76	12.87	12.0
2	D3	300	2.30	10.20	13.23	12.0
3	C2	150	2.49	12.10	14.87	12.0
4	C2	300	2.94	12.87	14.38	12.0
5	B3	150	2.30	10.08	13.97	12.0
6	B3	150	2.29	10.52	13.86	12.0
7	C1	150	2.74	9.82	13.77	12.0
8	C3	150	2.03	11.64	17.71	12.0
9	C3	150	2.08	11.80	17.68	12.0
2	D3	300	3.07	6.28	-	18.0
3	C2	150	3.15	8.45	11.13	18.0
5	B3	150	3.32	6.94	11.12	18.0
6	B3	150	2.96	9.25	11.45	18.0
7	C1	150	3.28	8.07	10.27	18.0
8	C3	150	2.73	8.05	13.08	18.0
9	C3	150	2.90	9.06	12.83	18.0

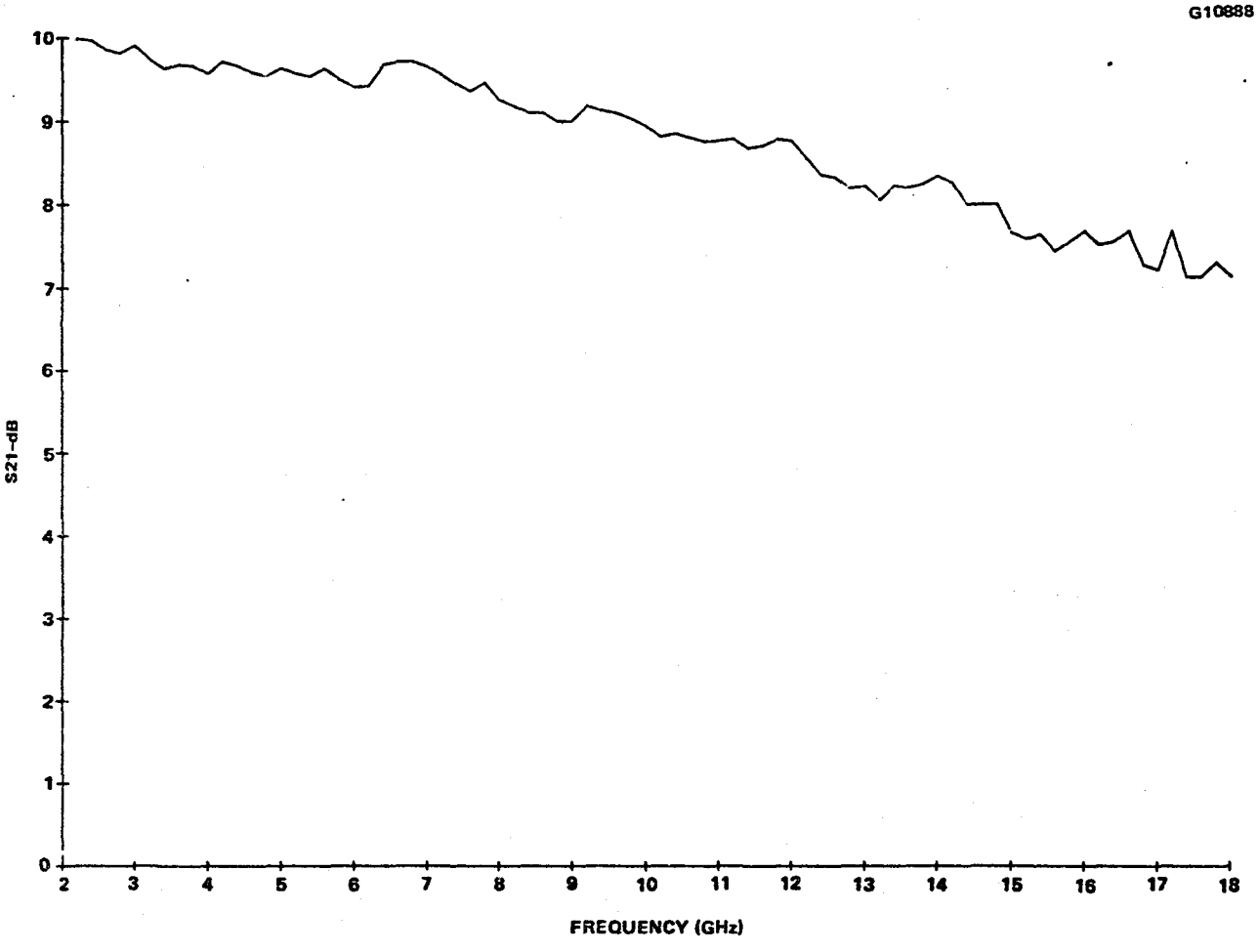


Figure 3-14 $|S_{21}|$ vs frequency for 0.25 x 150 μm gate FET.

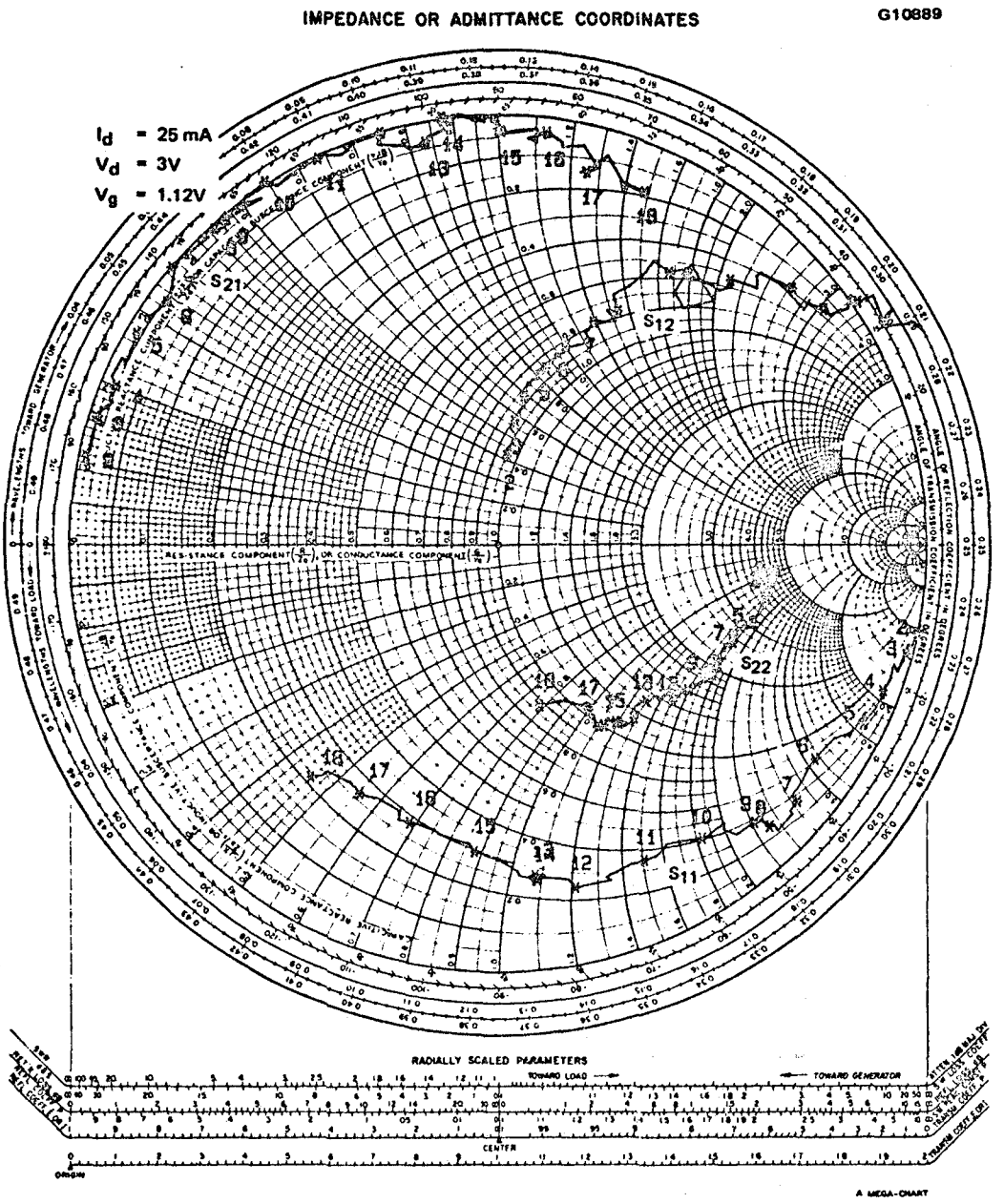


Figure 3-15 S-parameters of type B3 SM10 device (0.25 x 150 μm gate).

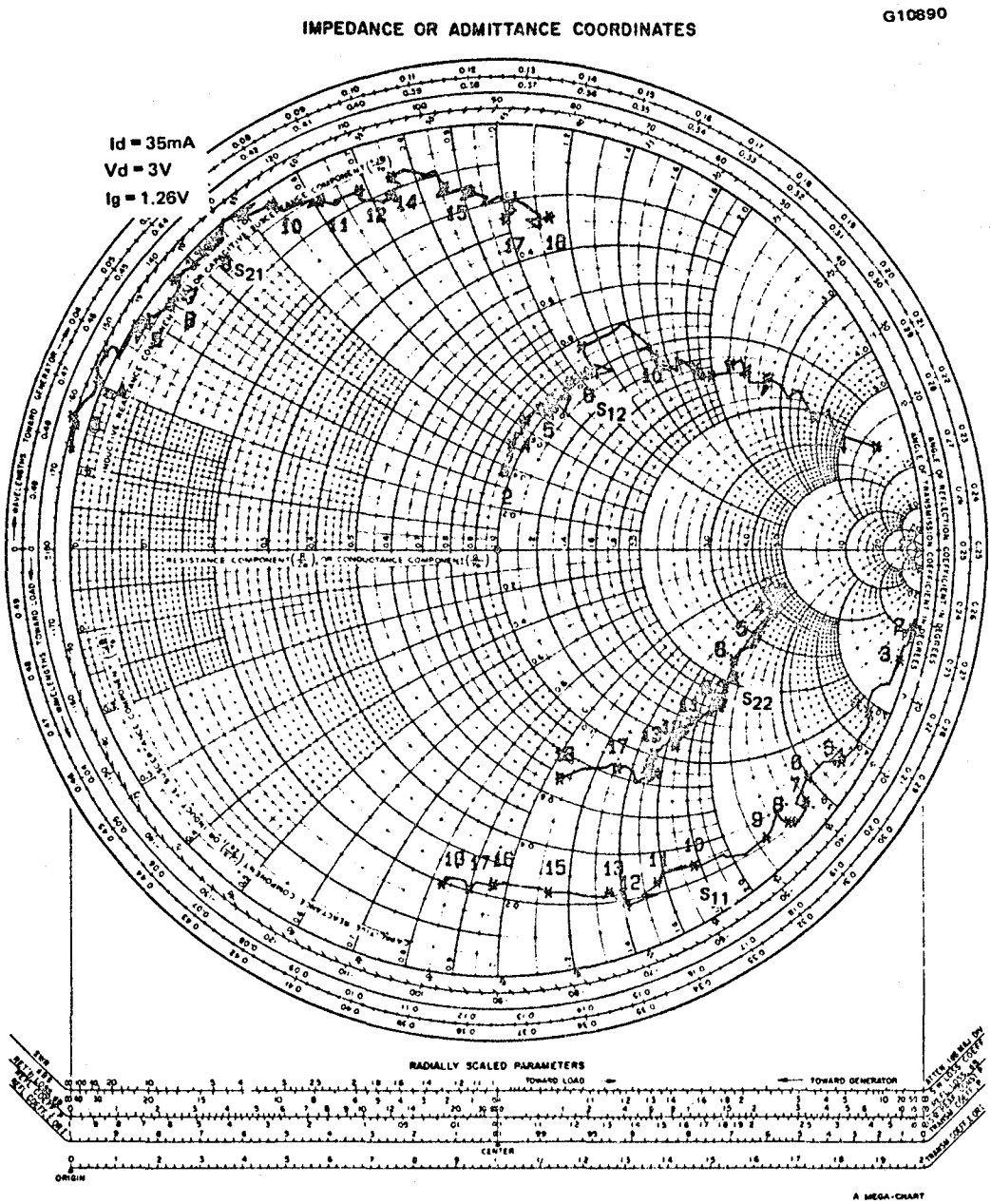


Figure 3-16 S-parameters of type C2 SM10 device (0.25 x150 μm gate).

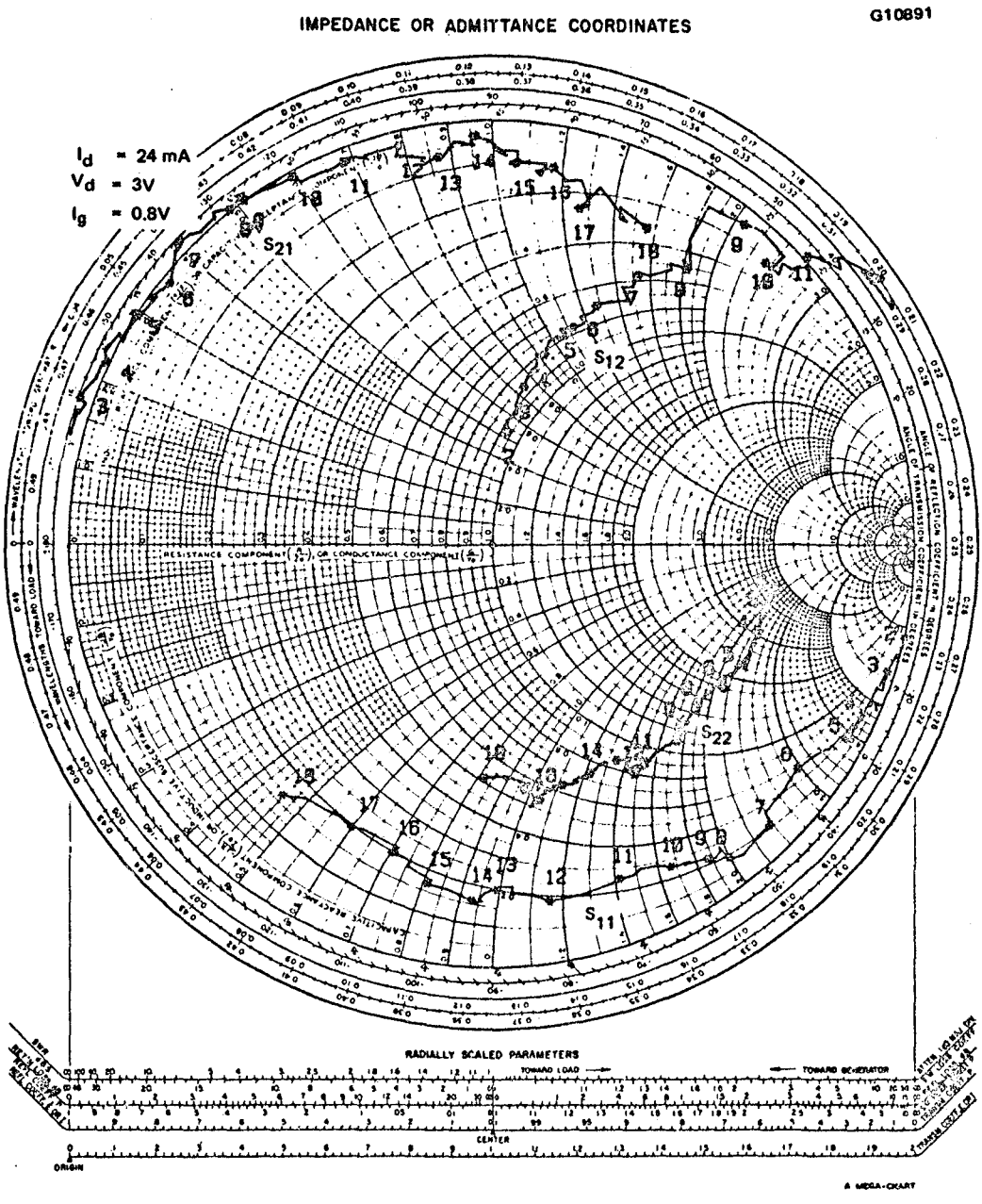


Figure 3-17 S-parameters of type C3 SM10 device (0.25 x 150 μm gate).

two 150 μm cells on a chip, but only one cell was used for the device characterization shown in Figure 3-15. The S-parameter data shown in these figures were obtained under low noise bias conditions.

The smaller gate width devices (75 μm per cell) such as types B1 and B2 did not yield good noise figure values at Ku-band frequencies due to noise matching difficulties. However, these small devices produced an excellent noise figure and high associated gain at higher frequencies. The best noise figure at 29 GHz, obtained from a 0.25x150 μm gate FET (lot SM08), is shown in Figure 3-18 as a function of the associated gain. This curve was obtained by first minimizing the noise figure and then by varying the drain bias current without changing the matching conditions. The best noise figure and associated gain at 29 GHz were 3.3 dB and 7.4 dB, respectively.

The equivalent circuit parameters of 0.25 μm gate and 0.5 μm gate devices are compared in Table 3-8. Representative devices from lots SM02 (0.5 μm) and SM08 (0.25 μm) with identical geometries (type B1) and a gate width of 75 μm were selected. The equivalent circuit element values were obtained from 2 to 18 GHz S-parameter data by computer data fitting techniques. Table 3-8 indicates that the values for the intrinsic capacitance such as C_{gs} and C_{gd} and gate transit time, τ , of the 0.25 μm gate device are, as expected, approximately half of those corresponding to the 0.5 μm gate device. However, the transconductance, g_m, of the 0.25 μm gate FET does not improve over that of the 0.5 μm gate FET. Also, the output conductance value, G_d, of the 0.25 μm gate FET is, as anticipated, considerably larger. However, the smaller capacitance values of the 0.25 μm gate FET can offset the G_d and g_m values more than enough to significantly improve the gain capability of the device at higher frequencies. The maximum available gain of these two devices are shown as a function of frequency in Figure 3-19. This figure includes other 0.5 μm gate FET results for comparison. The value of f_{max} , which is defined by the frequency where the MAG equals 0 dB, of the 0.5 μm gate FET at best reaches 70 GHz, while the 0.25 μm gate FET demonstrates an f_{max} of 93 GHz.

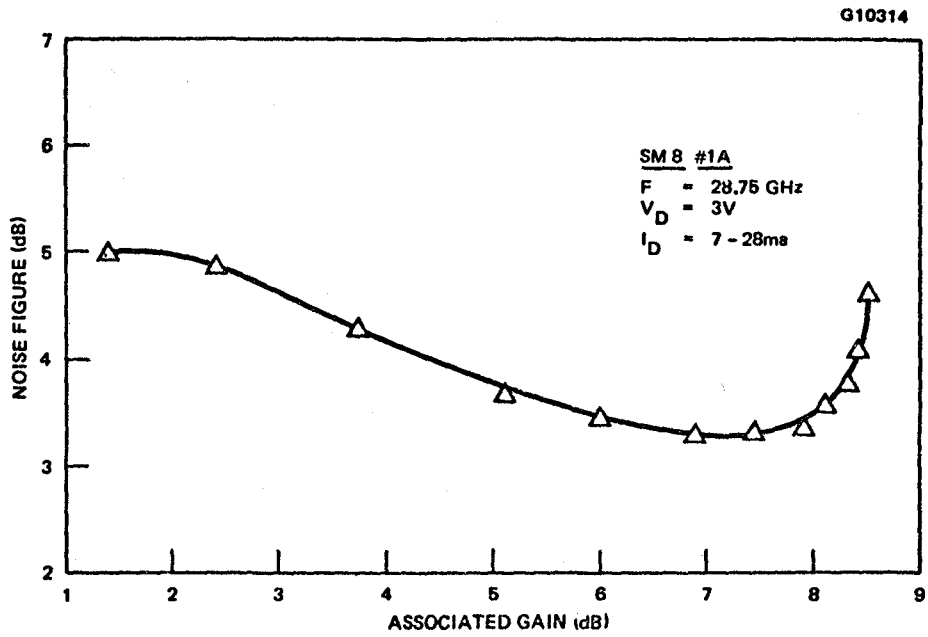


Figure 3-18 Noise performance of 0.25 μm gate device at 29 GHz.

TABLE 3-8

EQUIVALENT CIRCUIT ELEMENT VALUES
FOR 0.5 μm AND 0.25 μm FETs

Parameter	SM02 (0.5 μm)	SM08 (0.25 μm)
C_{gs}(pF)	0.0931	0.054
C_{gd}(pF)	0.0053	0.002
C_{dc}(pF)	0.0131	0.0091
R_i (Ω)	6.65	8.88
G_m (m℧)	12.08	11.0
τ(pS)	2.72	1.49
G_d(m℧)	0.848	1.53
L_g(pH)	366	344
R_g(Ω)	2.82	2.44
L_s(pH)	82.4	30.0
R_s(Ω)	2.63	3.17
L_d(pH)	172	303
R_d(Ω)	1.82	1.79
C_d(pF)	0.0396	0.0384

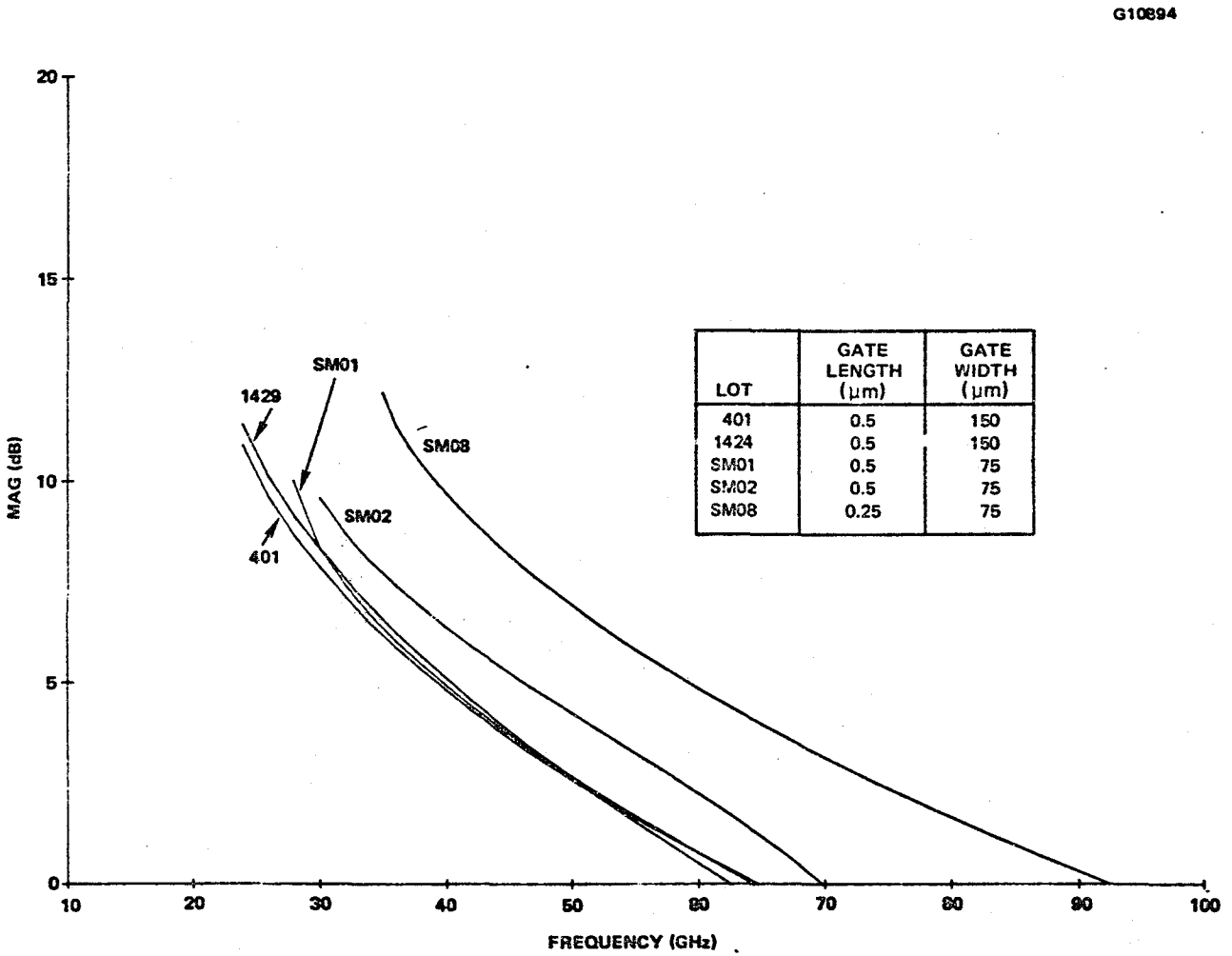


Figure 3-19 A comparison of the computed gain of the 0.25 μm and 0.5 μm gate devices.

3.2 DUAL-GATE FET

The dual-gate FET is a three port active device which can be used for mixing, gain control, phase shifting and amplification. Its properties have been examined both analytically and experimentally at frequencies ranging into Ku-band.[8-10] However, little work has been reported on devices and circuits operating at frequencies above 18 GHz.

3.2.1 Device Description

A conceptual sketch of the dual-gate FET is shown in Figure 3-20a. The two gates are located between the source and drain, allowing each to exercise control over the device operating current. A convenient representation for this device is a series connection of two single gate FETs as shown in Figure 3-20b. The first FET is operated in a common source configuration with its drain current feeding the source of the second FET. An SEM of our dual-gate FET is shown in Figure 3-21. Each gate finger is 0.5 μm in length and 75 μm wide resulting in a total gate periphery of 150 μm per chip. The gates are separated by a 1.5 μm spacing and are located in a 4.5 μm wide channel with gate 1 typically offset toward the source. A magnified view of the channel area is shown in Figure 3-21b. The overall chip size is typically 13x13 mils.

The same metallization systems and processing techniques used to fabricate the E-FET device, described in Section 3.1.2, are used to fabricate the dual-gate FET. The device is fabricated using our E-beam lithography system for all mask levels. During this program phase, five dual-gate FET lots were fabricated using both ion-implanted and VPE material for the active layer. The properties of each lot are listed in Table 3-9. Generally, the devices fabricated on the VPE material demonstrated superior performance as mixers at 30 GHz.

3.2.2 Dual-Gate FET I-V Characteristics

Depending on the bias conditions, the dual-gate FET is capable of operating in four different modes. The bias dependence of these modes, summarized in

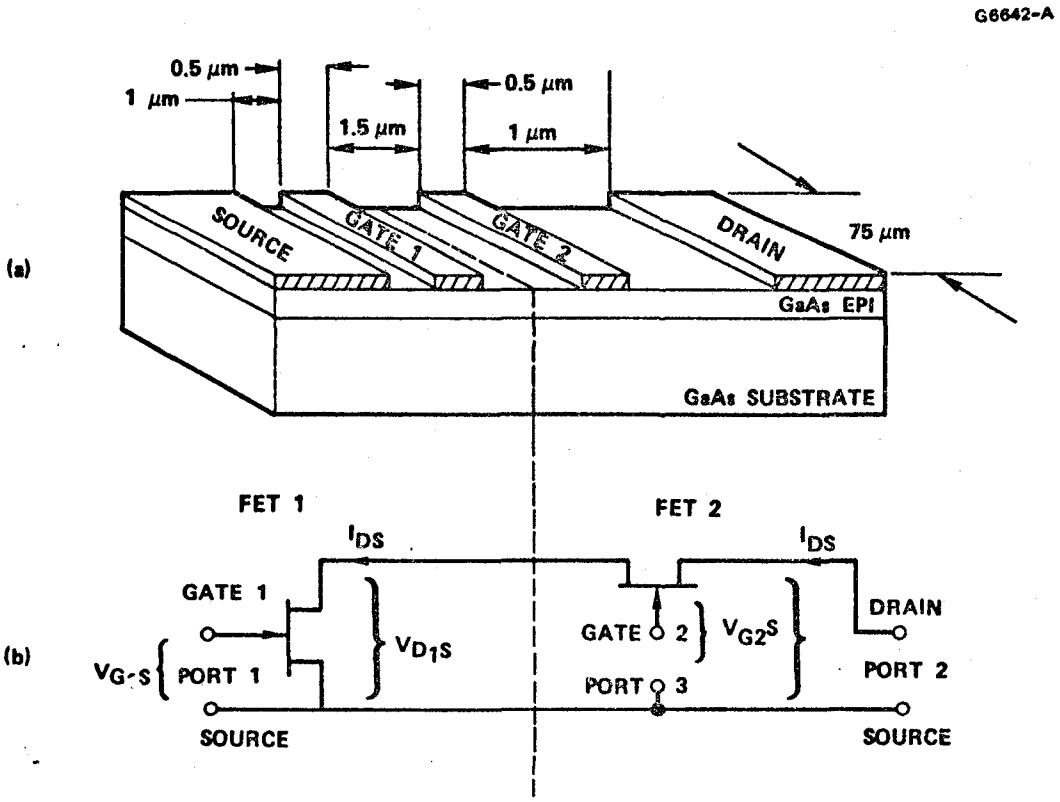
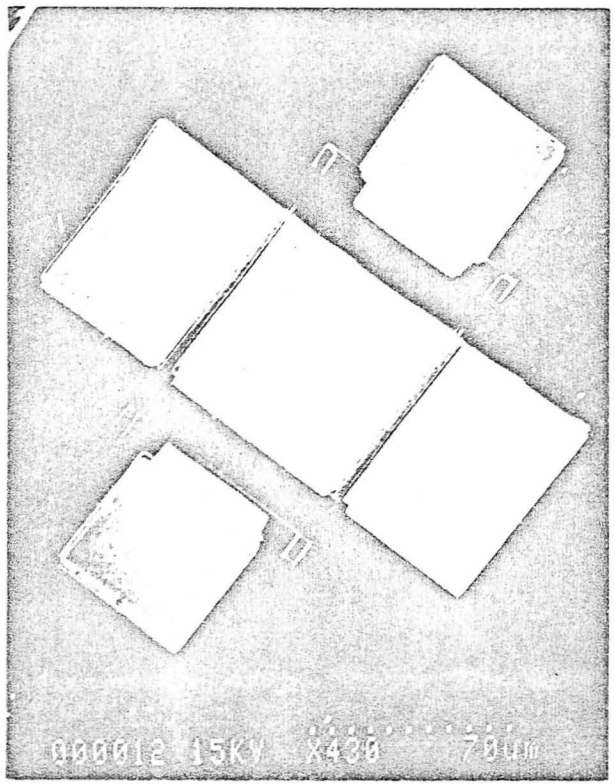
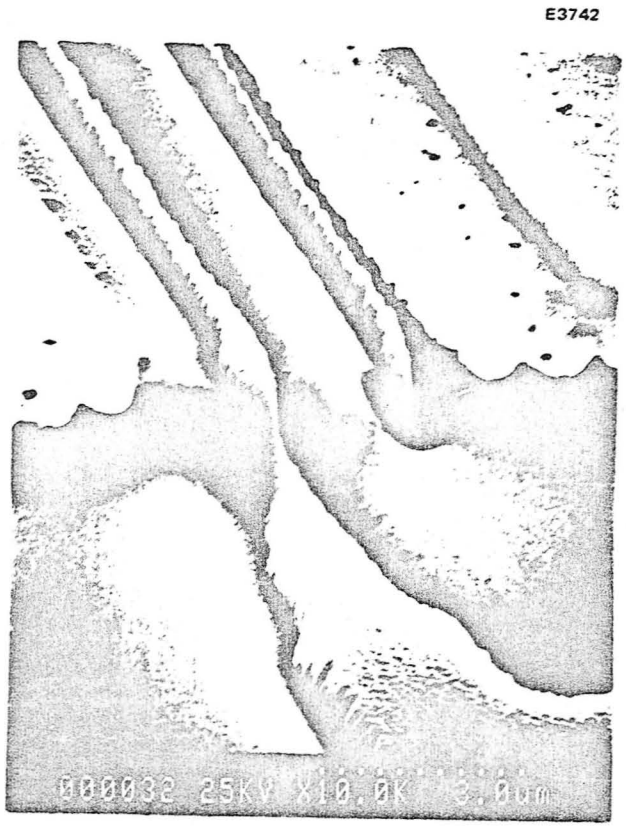


Figure 3-20 The dual-gate MESFET.



(a)



(b)

Figure 3-21 (a) E-beam fabricated half micron dual-gate FET.

(b) Magnified view of the channel area.

TABLE 3-9

DUAL-GATE FET LOTS

Lot	Material	Carrier Concentration, η (cm^{-3})
159	Ion Implanted	$3x10^{17}$
D2	Ion Implanted	$3x10^{17}$
D4	VPE	$1.9x10^{17}$
D5	VPE	$2.2x10^{17}$
D6	VPE	$2.6x10^{17}$

Table 3-10, can be understood by analyzing the device as two series connected FETs. The dual-gate FET I-V characteristics, shown in Figure 3-22, demonstrate the effect of the second control gate on the overall device operating characteristics. In each case V_{G2} was fixed and V_{G1} was varied 0.5 volts per step. The IR voltage drop across FET 1 will bias off FET 2 unless a positive voltage is applied to gate 2, as shown in Figure 3-22. The current control exercised by gate 2 is shown in Figure 3-23 where V_{G1} = 0 and gate 2 is varied in 0.5 volts per step.

The mixing action of a single gate FET is primarily the result of the modulation of the device transconductance, g_m. In a dual gate FET, the g_m of the first FET can be made to vary abruptly with the second gate voltage. The drain current as a function of the two gate control voltages is illustrated in Figure 3-24. The ability of gate 2 to control the gate 1 g_m can be easily seen from this curve.

TABLE 3-10

DUAL-GATE FET OPERATING MODES

Mode	FET I-V Characteristic	
	FET 1	FET 2
1	linear	linear
2	linear	saturated
3	saturated	linear
4	saturated	saturated

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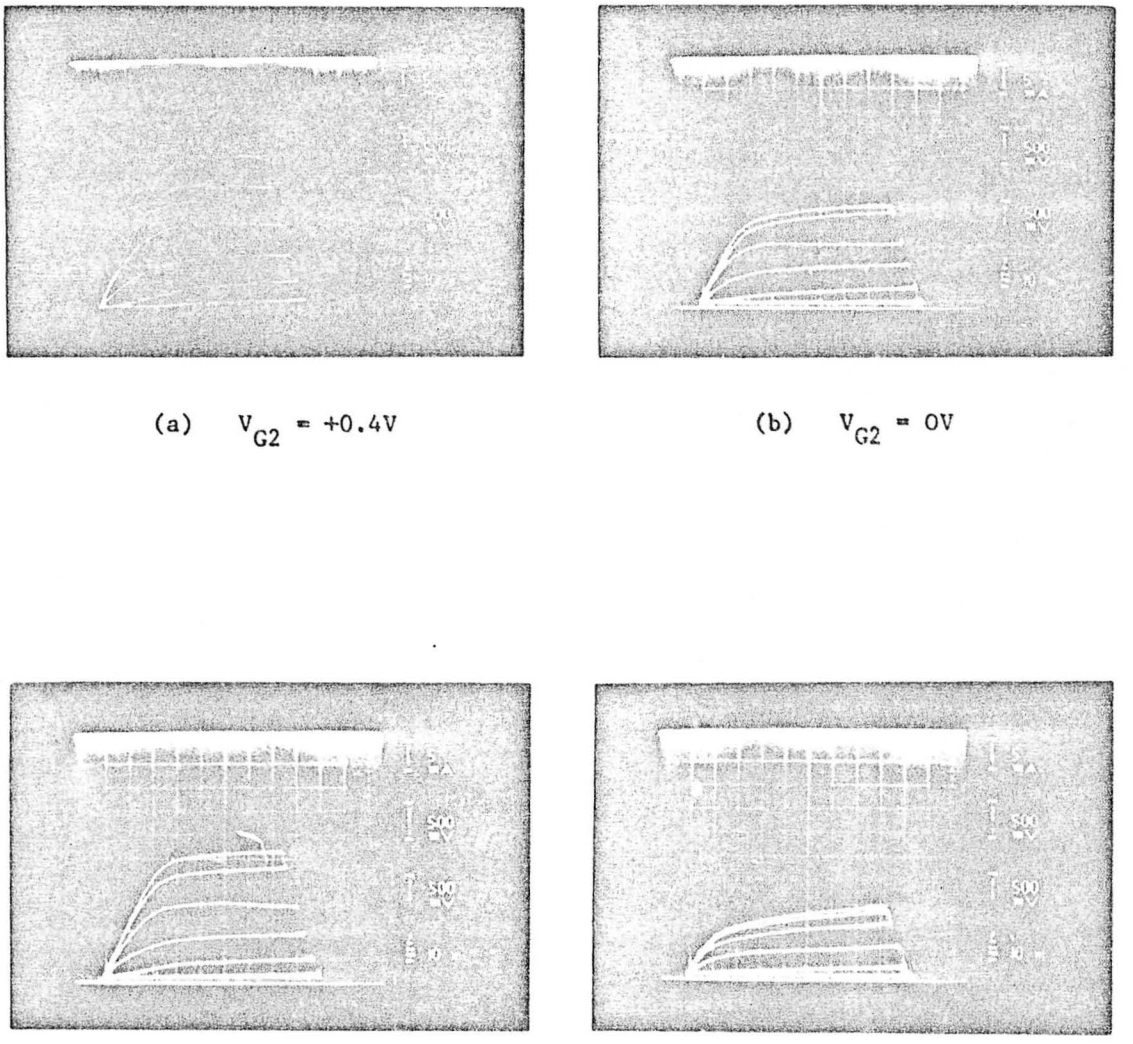


(a) V_{G2} = +0.4V

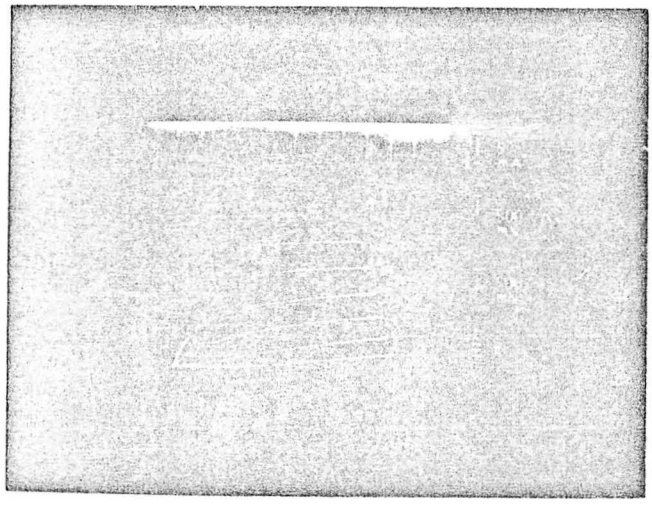
(b) V_{G2} = 0V

(c) V_{G2} = -0.5V

(d) V_{G2} = -1.0V

Figure 3-22 Dual-gate FET I-V characteristics, illustrating current limiting of second gate.

E4035



V_{G2} = 0 V

Figure 3-23 Dual-gate I-V characteristic for V_{G1} = 0; 0.5 volt steps on V_{G2}.

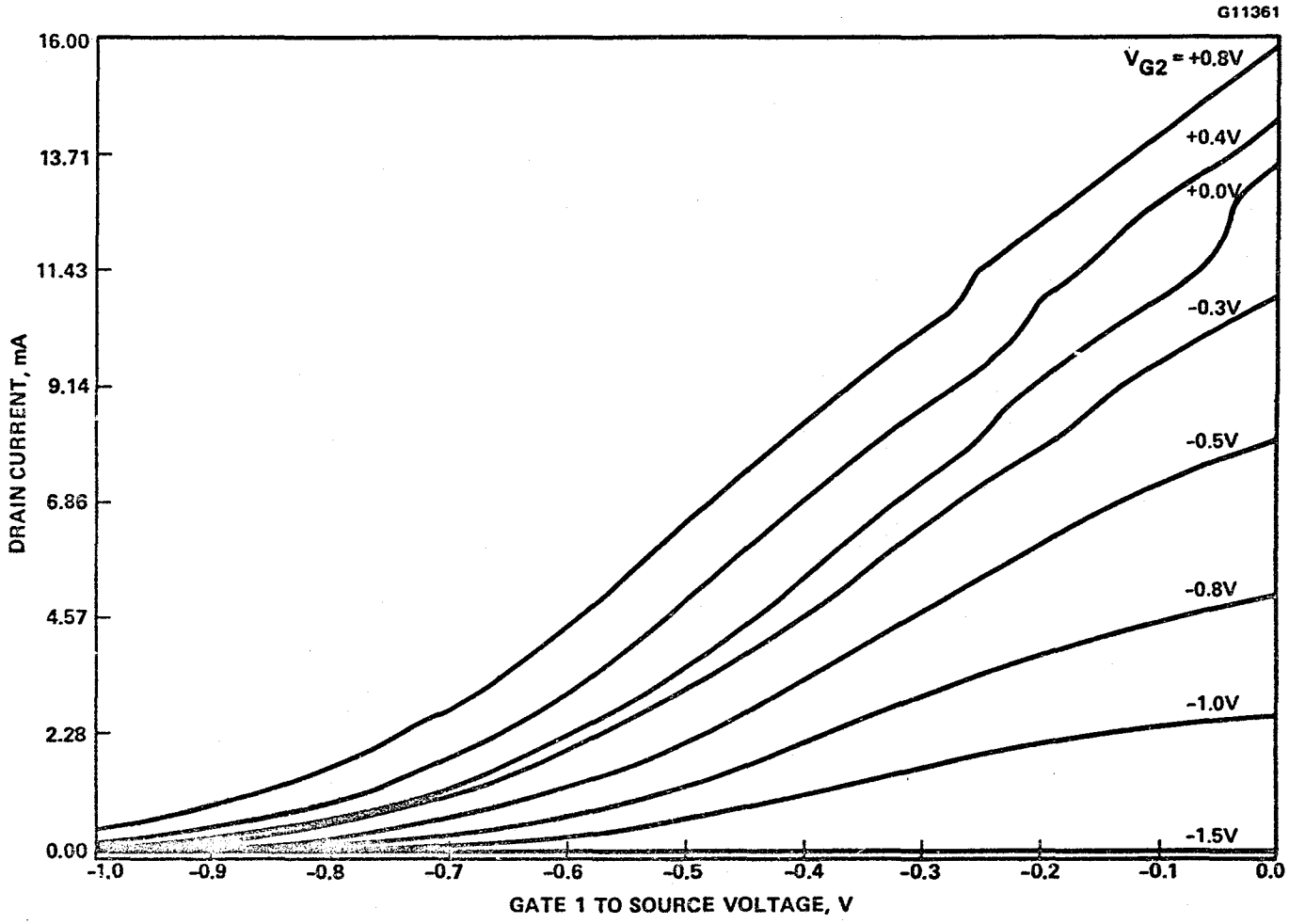


Figure 3-24 Device drain current as a function of gate 1 and gate 2 control voltages.

3.2.3 Device Characterization

Several devices were characterized from 2 to 18 GHz on our automatic network analyzer. To simplify the measurements, the three-port dual-gate device was measured with one of the ports terminated in a short circuit. The result with gate 2 shorted to ground is shown in Figure 3-25. In this configuration, the device is analyzed as a common source FET followed by a common gate FET. The frequency response as a function of V_{G1} is shown in Figure 3-26. The insertion loss is the highest for $V_{G1} = 0$, when gate 2 is controlling the current, making the g_m of gate 1 very low. The insertion loss is the lowest when gate 1 is negatively biased, $V_{G1} = -0.4$ V, and the g_m of gate 1 increased. The S-parameter data obtained with gate 1 grounded is shown in Figure 3-27.

The small signal equivalent circuit model of the cascode connected dual-gate FET device is shown in Figure 3-28. Due to its complexity, we did not attempt to "fit" the model to the measured data, but instead, created simple one port equivalent circuit models to use in the mixer circuit design efforts. The simplified models and element values are shown in Figure 3-29.

Typically, the noise figure of a dual-gate FET is considerably higher than that of a single gate device due to the additional noise generators in the "second" FET. The noise performance of the dual-gate FETs with gate 2 grounded was measured at 12 GHz for some early lots. The noise figure was typically 4.1 dB with 9.25 dB associated gain.

We experienced several device failures with devices from lot D5. SEM and X-ray analysis were performed and the test results are presented in Appendix B. The problem appears to be unique to the D5 lot since such failures have not reoccurred.

3.2.4 Summary

As a result of this program, Hughes has developed E-beam lithography processes for the fabrication of dual-gate FETs, which are currently being applied to Ku-and Ka-band mixers. This program has demonstrated the viability of 0.5 μm dual-gate FET geometries for mixer applications at frequencies up to 30 GHz.

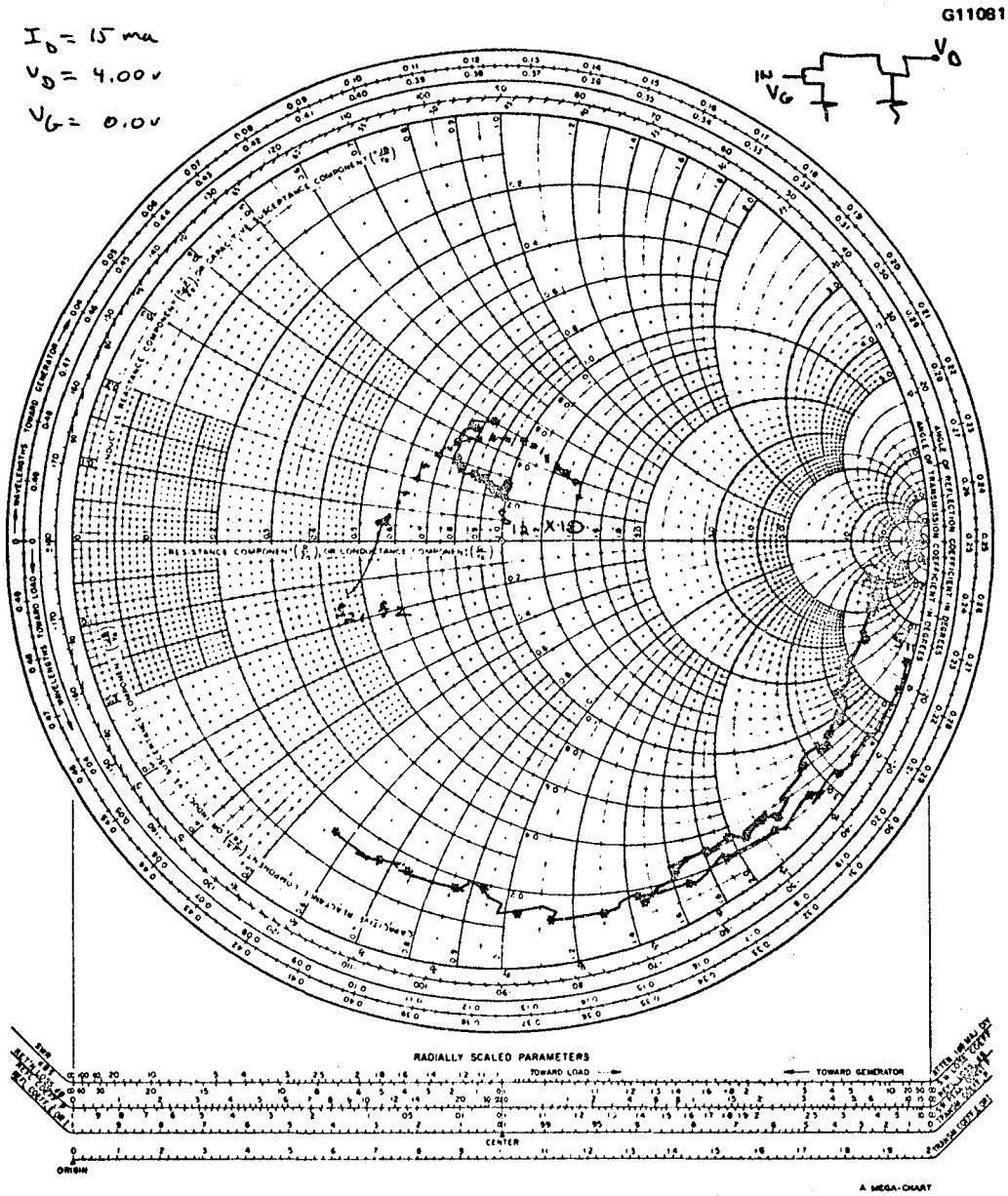


Figure 3-25 Dual-gate MESFET, gate 2 grounded.

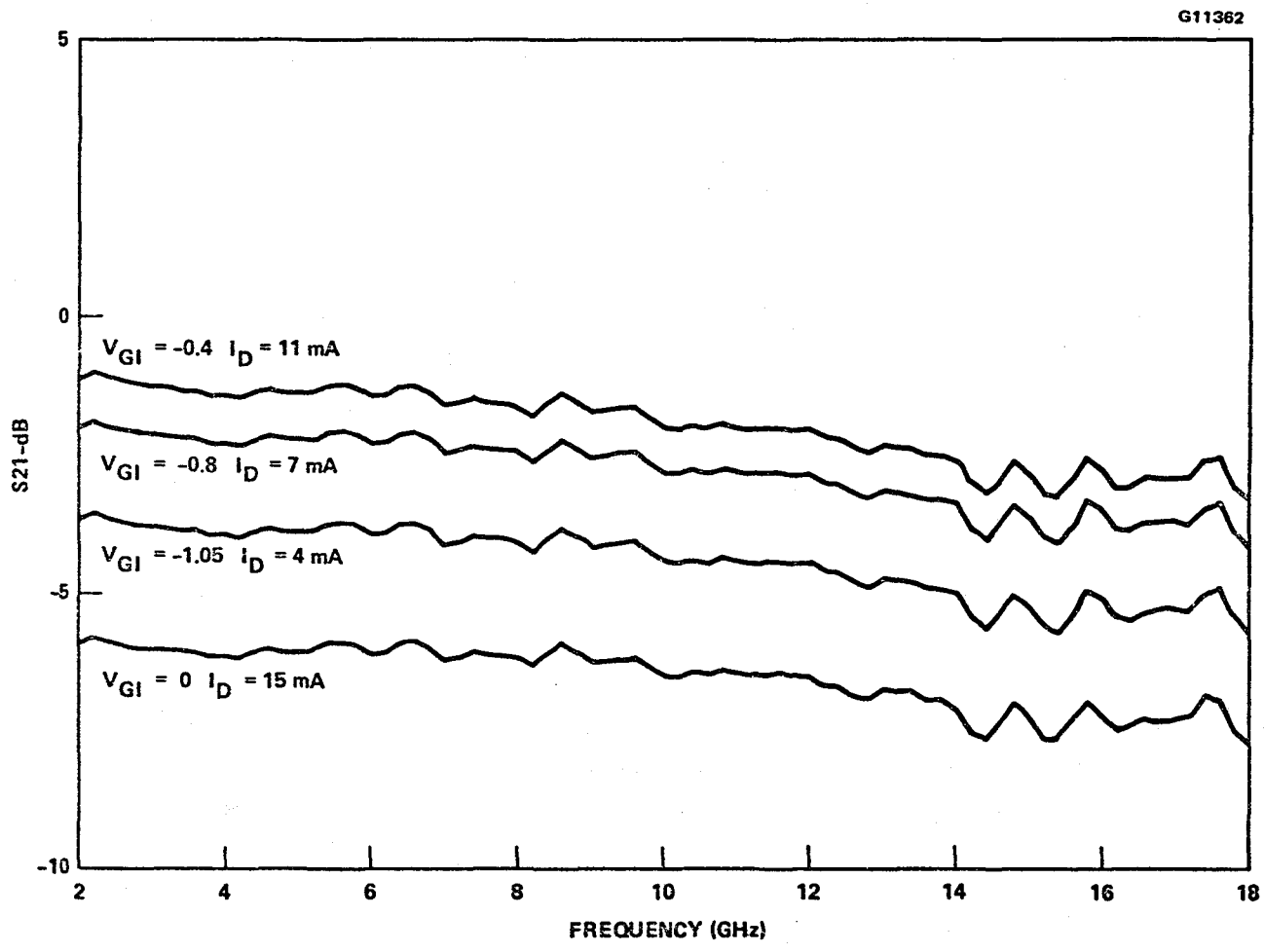


Figure 3-26 Insertion gain of cascode dual-gate FET as a function of gate 1 voltage.

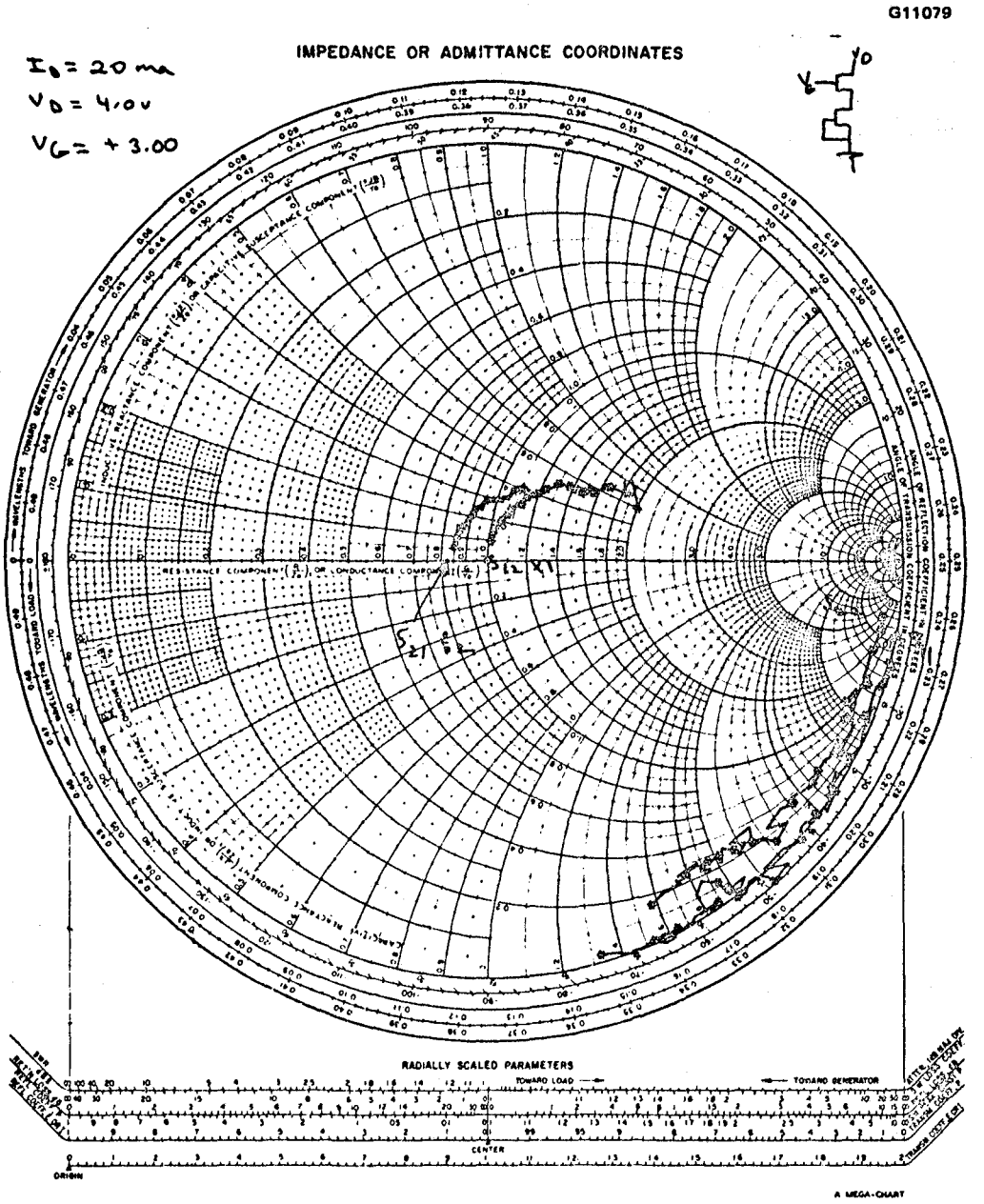


Figure 3-27 Dual-gate MESFET, gate 1 grounded.

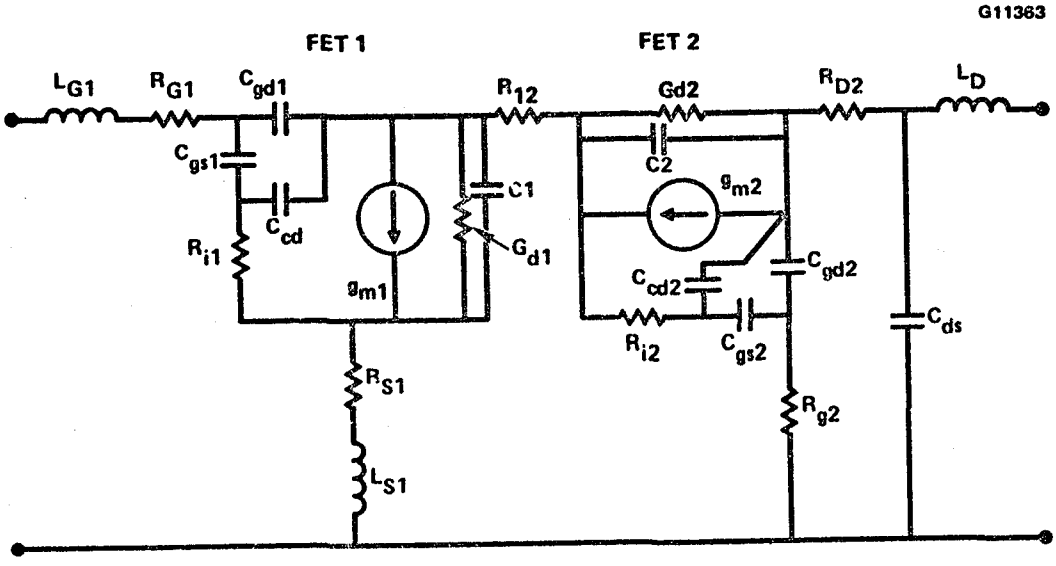


Figure 3-28 Two-port equivalent circuit representation of dual-gate device with gate 2 grounded.

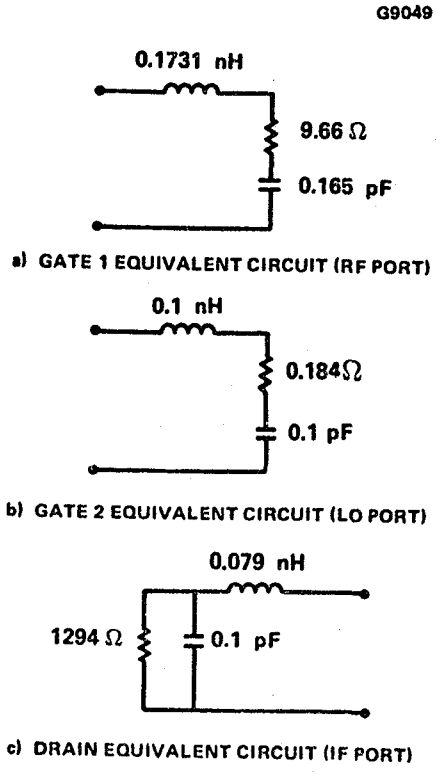


Figure 3-29 Simplified dual-gate equivalent circuits.

3.3 OSCILLATOR FET

The predominate source of oscillator phase noise is upconverted 1/f baseband noise in the device. Hence, the problem of minimizing the oscillator phase noise can be reduced to minimizing the device 1/f baseband noise. Typically, GaAs FETs have very high 1/f noise with a corner frequency of several hundred MHz. The origin of this noise appears to be traps located within the active channel layer as well as at the epi-substrate or epi-buffer layer interface. These traps modulate the source-gate depletion layer capacitance, thereby generating drain current fluctuations. Measurements by Pucel[11] and others indicate that the 1/f noise both increases and decreases with drain current depending on the bias conditions and temperature. This result suggests that the trap distribution is not uniform but, more likely, segregated at narrowly defined physical regions, for example, the interface region between the active layer and the semi-insulating substrate.

3.3.1 Device Description

The device selected for the FET LO development is shown in Figure 3-30. The overall chip size is 18x22 mils. The device is a 300x0.5 μm low noise FET with all mask layers, with the exception of the gate, fabricated by photolithography. The 0.5 μm gate is defined by using electron beam lithography techniques. The source and drain ohmic contacts are formed by using an Au-Ge/Ni/Au metallization system. The source-drain spacing is 2.9 μm. A metallurgical barrier metal of chromium and palladium is employed to separate the aluminum gate from the gold bonding pad, thus avoiding the formation of intermetallic compounds. This metallization system has proven to be reliable in numerous life tests. The device has been optimized for low noise common source operation at X and Ku-band frequencies.

3.3.2 Noise Properties

The flicker noise (1/f noise) properties of FET devices fabricated on ion implanted and VPE material were evaluated in an effort to determine the best material for the oscillator device. The tests were conducted with the devices mounted in a common source configuration. The noise properties of the devices were compared by measuring the low frequency (DC to 10 kHz) drain current

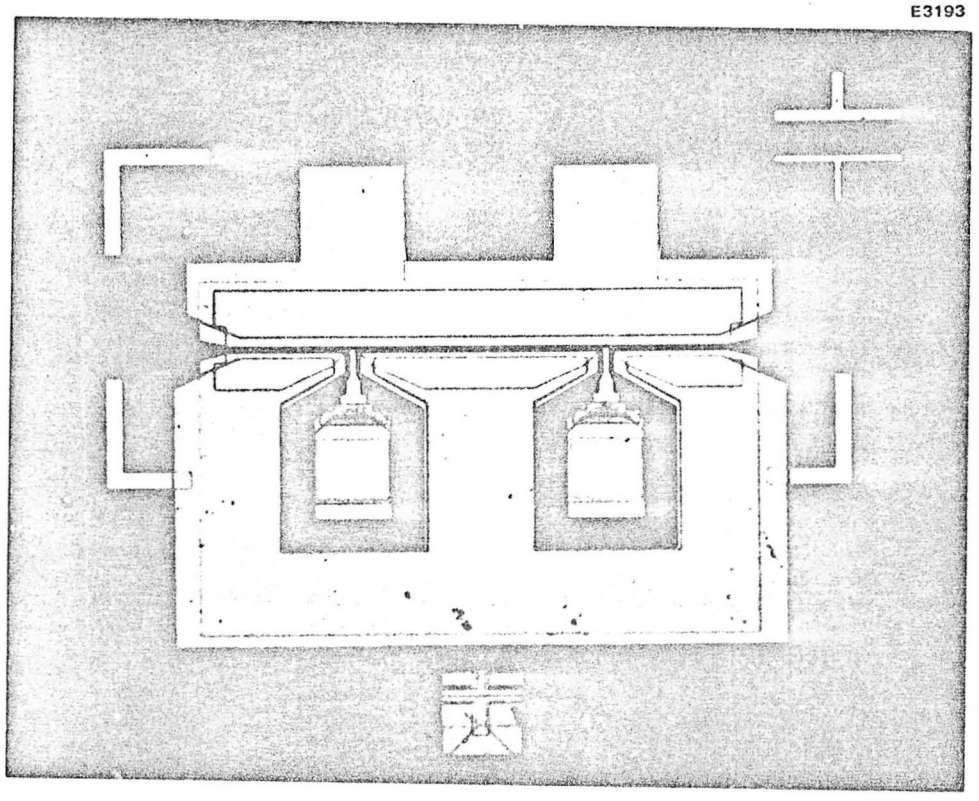


Figure 3-30 Hughes standard 0.5x300 μm PI-300 low noise FET.

fluctuations of each device operating at a 3 volt drain-source voltage and a drain current of 10.0 to 20.0 mA. The small number of measured test samples prevented the determination of the optimum material properties. However, of the devices studied, those fabricated with VPE material consistently demonstrated lower drain current fluctuations. The drain noise current versus baseband frequency for a VPE and ion implanted device operating at 3 volts and 20 mA is shown in Figure 3-31. As illustrated in the figure, the VPE device demonstrated lower noise current fluctuations than the ion implanted device at any frequency. At 5 kHz the mean squared drain current fluctuation is 2.7 nA^2/Hz for the VPE device, compared to 42 nA^2/Hz for the ion-implanted device. These results are not fully understood and will be the subject of future investigations.

3.3.3 Common-Gate Circuit

The devices used in the oscillator development were selected from Lot L191 which was fabricated with VPE material with a doping concentration of $2.4 \times 10^{17} cm^{-3}$. The common source 2 to 18 GHz S-parameters of a typical L191 device are shown in Figure 3-32. Based on these S-parameters, small signal equivalent circuit element parameters were computed from the data and are listed in Table 3-11. Using this small signal model, a simple common gate circuit was analyzed to determine the frequency range over which negative resistance could be generated. The circuit, shown in Figure 3-33, generates negative resistance by employing a combination of internal and external feedback sources consisting of device interelectrode capacitances and gate bond wire inductance. The bond wire inductance was included as part of the device model. Several different combinations of source to gate inductance were examined and two examples are shown in Figure 3-32. With ℓ = 0.18 nH, this circuit generated a negative resistance extending from 21 to 30 GHz with a maximum value of -3.99 ohms at 24 GHz. The negative resistance versus frequency is also shown for ℓ = 0.28 nH and demonstrates the degree of control which is available for optimizing the frequency range and the negative resistance peak. These results indicate that this device and circuit are suitable for use in the 25 GHz LO development.

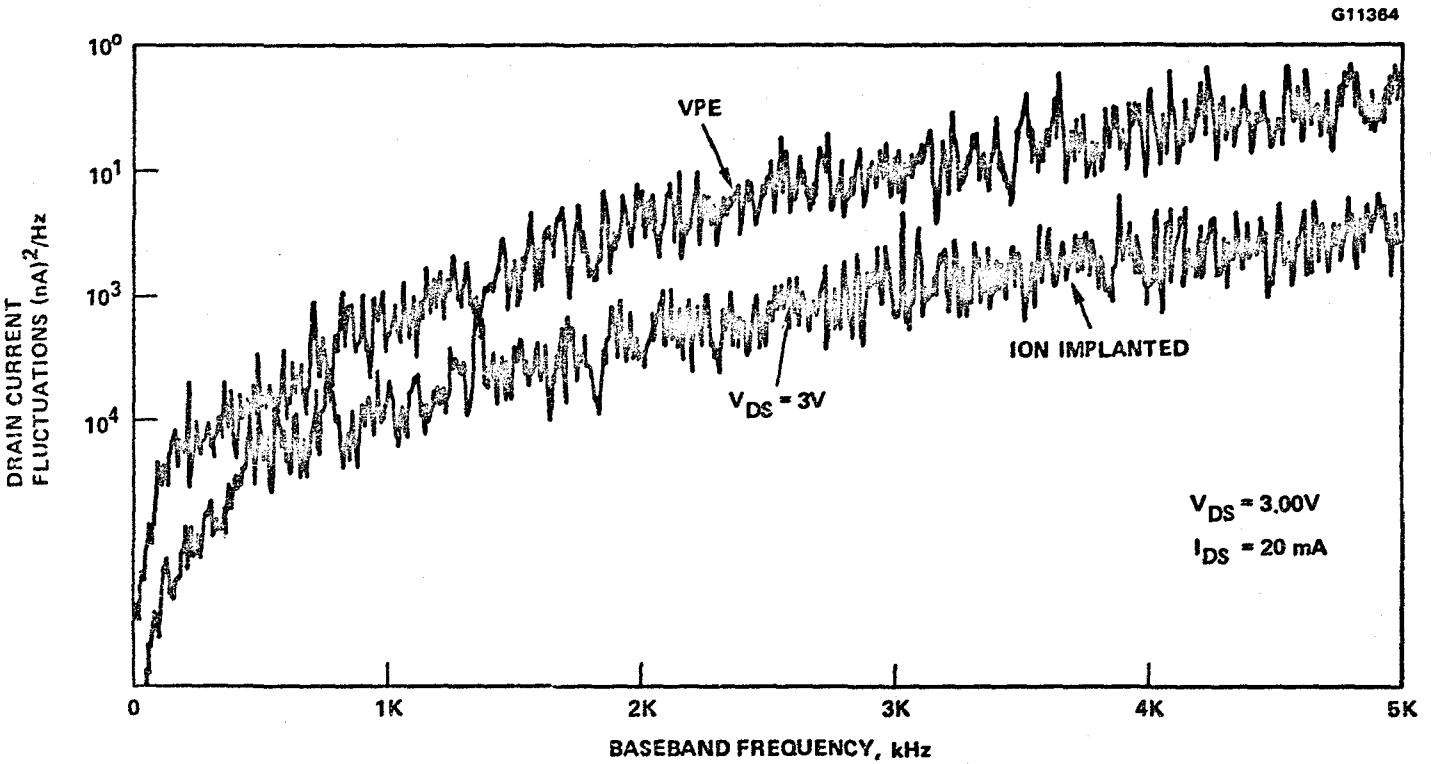


Figure 3-31 Drain current fluctuations versus frequency.

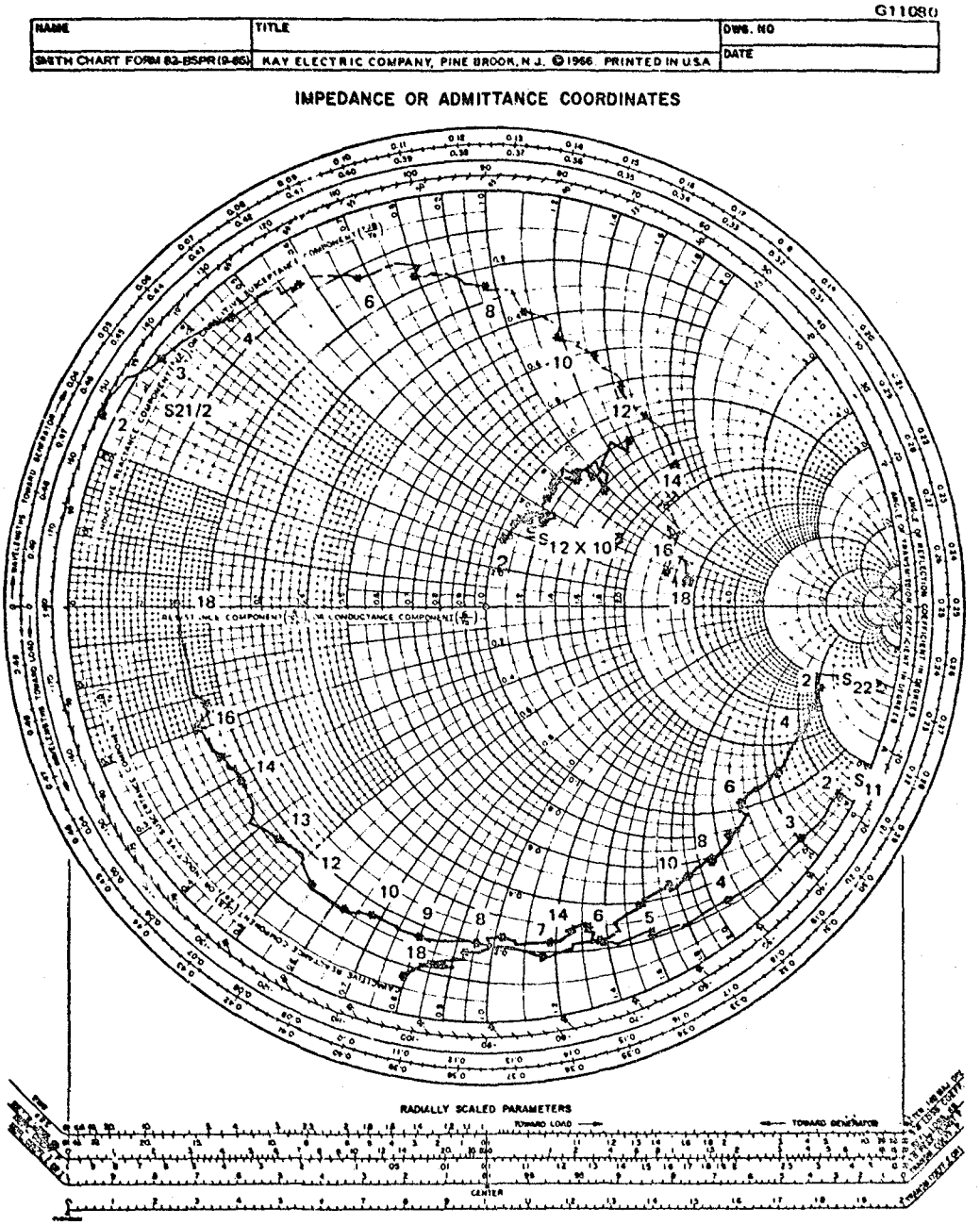


Figure 3-32 Common source S-parameters of L191 device.

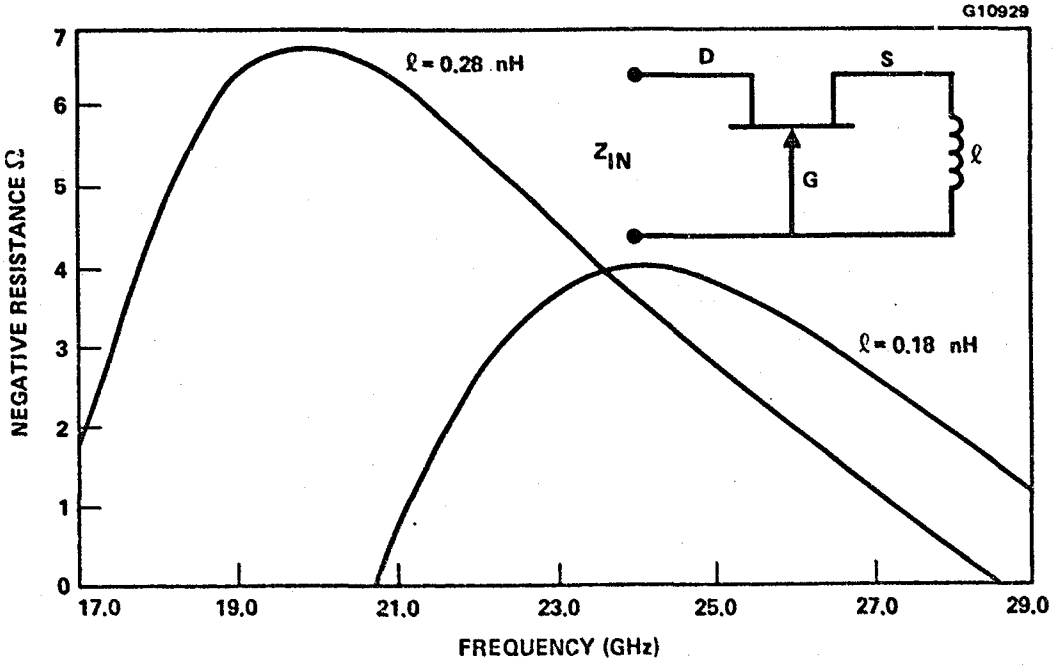


Figure 3-33 Common gate circuit negative resistance versus frequency.

TABLE 3-11

EQUIVALENT CIRCUIT ELEMENT
VALUES FOR TYPICAL L191 DEVICE

Circuit Element	Value
R_i (Ω)	1.4
C_{gs} (pF)	0.32
C_{gd} (pF)	0.062
C_{dc} (pF)	0.01
gm (m℧)	55.0
T (pS)	2.36
G_d (m℧)	4.7
C_{ds} (pF)	0.06
R_s (Ω)	1.27
R_g (Ω)	2.5
R_d (Ω)	1.9

3.3.4 Summary

The oscillator circuits constructed with these devices satisfied all the program requirements with the exception of the phase noise. The device periphery, voltage, and current capabilities were sufficient to satisfy the oscillator output power requirements. As described in Section 4.4, the voltage and temperature sensitivity of the device were suitable for the oscillator design goals. While the oscillator phase noise goals were not achieved, by optimizing the material properties, we anticipate significant future improvements in the phase noise performance of the devices.

4.0 RECEIVER COMPONENTS

4.1 LOW NOISE AMPLIFIER DEVELOPMENT

This section discusses the development of the low noise amplifier (LNA). The general design considerations will be reviewed first followed by the amplifier description and equivalent circuit. The results obtained on the single and multistage units will be presented and summarized. Finally, the results obtained on cryogenically cooled units will be discussed.

4.1.1 General Design Considerations

The design goal for the single stages of the LNA includes a 3.5 dB noise figure with a minimum associated gain of 6 dB from 27.5 to 30 GHz. The most difficult specification to achieve was the 3.5 dB noise figure since a new state-of-the-art device had to be developed to realize this goal. This device development is described in Section 3.1.

4.1.1.1 Amplifier Configuration - The two major configuration alternatives for the individual stages are the balanced and single-ended configurations as indicated in Figure 4-1. The balanced structure uses two transistors with a quadrature hybrid at the input and output to split and recombine the RF power. The balanced configuration has several features which make the increased cost and complexity worthwhile in many applications, including increased power handling capability and built-in isolation.

Since the input power is split between two transistors, approximately twice as much power can be handled by the balanced stage. The isolation is provided by the matched termination at the fourth port of the hybrid. Assuming the hybrid is ideal and the mismatch of the transistors is identical, all the power reflected back by the FETs is absorbed by the termination. The same situation exists at the output, so no additional interstage isolation is normally required to prevent excessive ripple in multistage broadband applications.

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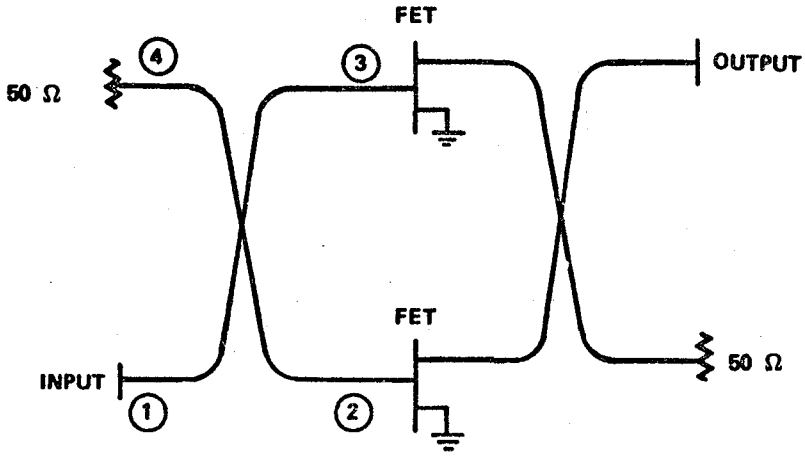
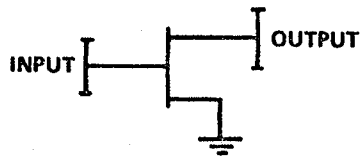


(a) BALANCED CONFIGURATION



(b) SINGLE-END CONFIGURATION

Figure 4-1 Balanced and single-ended FET gain stages.

The single-ended gain stage has no built-in isolation. In narrow bandwidth designs, typically two or three stages can be cascaded directly without too much difficulty. However, for wide bandwidth applications, interstage isolation is required to prevent excessive ripple or stability problems. Ferrite MIC isolators with near octave bandwidths have been demonstrated at frequencies up to 26.5 GHz, and similar devices are possible for Ka-band with some development. The single-ended approach generally has the advantages of lower loss and simplicity.

The choice between a balanced or unbalanced approach for the low noise amplifier is clearly a choice between development of a quadrature hybrid or isolator for 30 GHz. Very wideband designs below 18 GHz have generally used the balanced structure due to the isolator bandwidth limitations relative to an overcoupled (less than 3 dB) interdigital coupler design. We chose the single-ended approach to provide superior performance and simplicity due to the narrow bandwidth requirements and the small number of stages to be cascaded.

4.1.1.2 FET Matching Network Design - The matching networks in a low noise FET amplifier determine the amplifier bandwidth, control the gain magnitude and flatness, and minimize the noise figure over the desired band. The noise figure of an FET gain stage is largely controlled by the input matching network while the output matching network primarily affects gain and output power capability. The matching requirements at the input for minimum noise and maximum gain are generally not compatible. A compromise must be made between gain and noise figure in the design. A figure of merit for a gain stage which can be helpful in optimizing the noise figure of an amplifier with a large number of stages is the noise measure M defined by

$$M = F + \frac{F - 1}{G_a - 1} \qquad (4.1\text{-}1)$$

where F is the noise figure of a stage and G_a is its associated gain. The significance of the noise measure is that it is the noise figure of an infinite cascade of identical stages.

If all stages in a high gain multistage amplifier were designed to be identical, the optimum noise figure would be achieved by minimizing the stage noise measure, not the stage noise figure. In practice, the first one or two stages of a FET amplifier will be biased for lower noise measure, but the following stages can be identical and biased for higher gain. The optimum design of the early stages depends on the functional relation between noise figure and gain for the FET used. This becomes a rather complex design problem to approach analytically. To do so requires a detailed knowledge of the device S-parameters and noise parameters. In practice, a low noise design is optimized empirically using an approximate analytical computer-aided design as the starting point.

The device equivalent circuit model, for one of our 0.5x100 μm gate width FETs biased for low noise, is shown in Figure 4-2. The element values of this model were derived from device S-parameter measurements in the 2 to 18 GHz band by using computer optimization techniques to "fit" the model to the S-parameter data. The terminal inductances shown in the figure are bonding lead inductances.

This equivalent circuit forms the basis of our matching network design. Since direct measurement of device S-parameters at 30 GHz is not currently possible, we must rely on indirect methods to generate the data required for the amplifier design. Hence, we employ the device equivalent circuit model to generate S-parameter data at 30 GHz. While the model is strictly valid only over the 2 to 18 GHz frequency range, since it is based on a physical representation of the device, it can be extended to frequencies above 18 GHz with reasonable accuracy.

For the actual matching network synthesis, the 14-element model is simplified to the unilateral model approximation shown in Figure 4-3 where the element values have been optimized to fit the equivalent circuit model over the band of interest. Note that the shunt and series feedback elements have been eliminated. With this unilateral model approximation, the input and output matching networks can be addressed independently. Once the network topology and approximate element values are derived using the unilateral model, the design can be refined using computer-aided design (CAD) techniques. In the CAD optimization, the complete 14-element model, including the effects of feedback, is used.

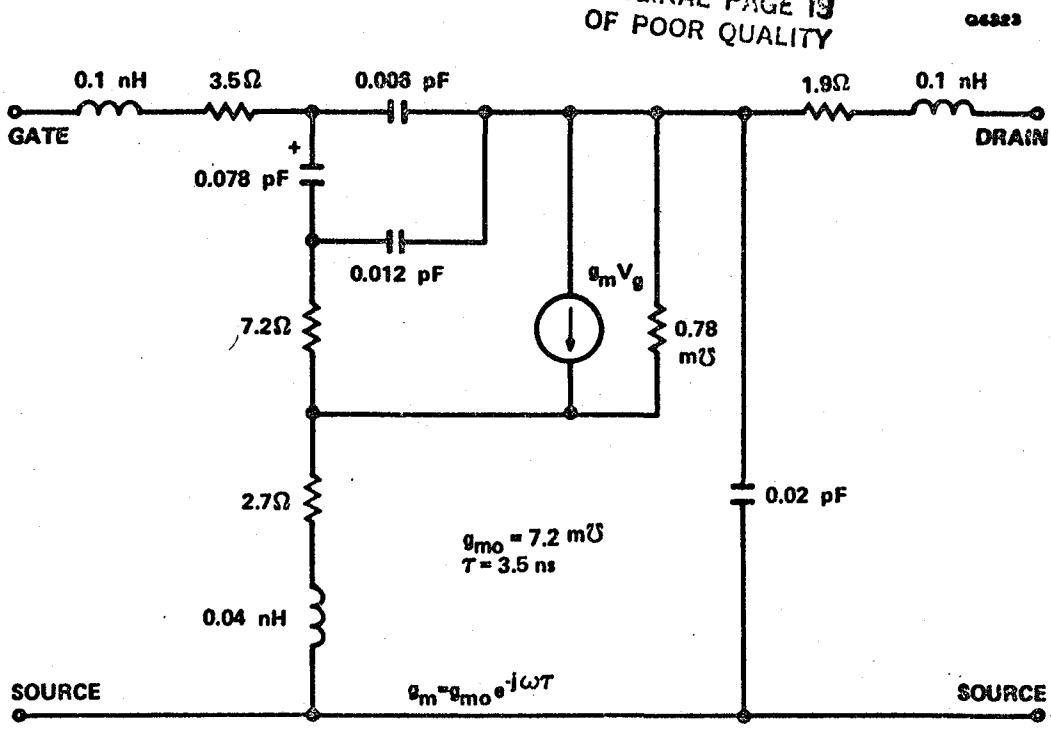


Figure 4-2 Equivalent circuit model of 100 μm gate width FET.

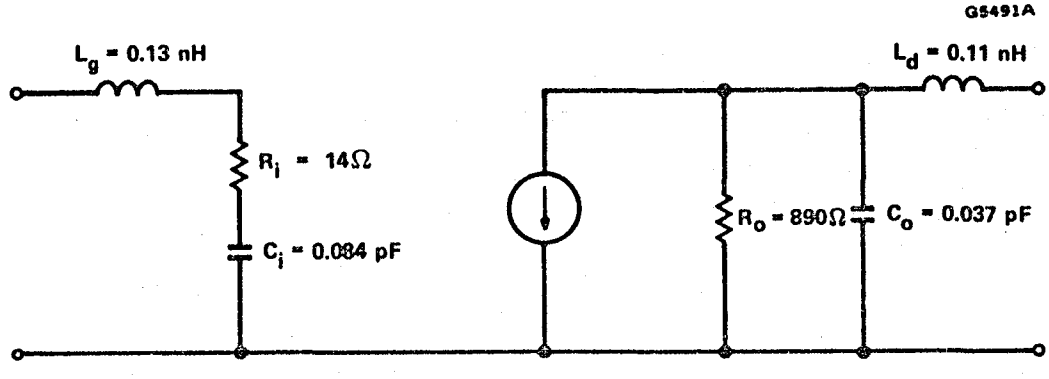


Figure 4-3 Unilateral model approximation.

The series input/output inductances are bonding lead inductances which can be controlled by the device-circuit interface. The basic matching circuit limitation is determined by the inherent device input/output Q's defined by

$$Q_i = \frac{1}{\omega_o R_i C_i} \tag{4.1-2}$$

for the input and

$$Q_o = \omega_o R_o C_o \tag{4.1-3}$$

for the output. These parameters determine the relation between bandwidth, maximum mismatch over the band and required matching network complexity.

The matching problem for optimizing noise figure over a given bandwidth is very similar to that of matching for maximum gain. The conjugate of the optimum source impedance for minimum noise can be approximated by a series RC circuit with constant element values C_{in} and R_{in} over a broad frequency range. The capacitance C_{in} is approximately the same as the input capacitance C_i in the unilateral model. The resistance R_{in} is typically much higher than R_i which means that the input Q for optimum noise matching is significantly lower than the actual device Q. This implies that a simpler, broader bandwidth matching network can be used for noise matching.

Before considering the actual matching network design, it is appropriate to consider the limitations imposed by the Q-bandwidth product. An important property of matching networks is that it is possible to perfectly match a complex load (Q>0) to a source at only a finite number of discrete frequencies, and not over a band of frequencies. This is a result of the Bode[12] - Fano[13] network limitation which can be expressed as

$$\int_0^\infty \ln \frac{1}{|\Gamma(\omega)|}\, d\omega \leq \frac{\pi \omega_o}{Q} \tag{4.1-4}$$

where $\Gamma(\omega)$ is the input reflection coefficient of the passive lossless network coupling the load to the source, ω_o and Q are the resonant frequency and the Q of the load, respectively. The equality sign holds providing $\Gamma(\omega)$ has no zeros in the right-half complex plane. The above equation illustrates that a low reflection coefficient can be obtained only over a limited bandwidth. In fact, the most efficient network would provide a constant input reflection coefficient ($|\Gamma|(\omega) = |\Gamma_m|$) over the desired bandwidth, and totally reflect incident power outside of this bandwidth. For this ideal matching network, the in-band reflection coefficient is given by Equation (4.1-4) as

$$|\Gamma_m| = e^{-\pi/wQ} \qquad (4.1\text{-}5)$$

where $w = \Delta\omega/\omega_o$ is the desired normalized bandwidth.

The characteristic described by Equation (4.1-5) cannot be realized in practice since it requires a matching network with an infinite number of elements. However, it is possible to approximate this rectangular shaped passband characteristic with a reasonably small number of elements.

Figure 4-4 illustrates the maximum in-band transmission loss as a function of the Q-bandwidth product with network complexity as a parameter. This curve was derived from Fano's work with low-pass matching networks. The parameter "n" represents the number of poles in the complex plane, and for a given number of poles, Fano's network is optimum in the sense that the maximum value of the reflection coefficient is a minimum. It is interesting to note that increasing the matching network complexity from a single pole to a double pole network produces the greatest improvement in the transmission loss, and that little is to be gained for the added circuit complexity beyond n = 3.

4.1.1.3 Matching Network Topology - The design considerations discussed above can be used to determine the input matching network. In the unilateral device approximation, the input impedance to be matched for optimum noise figure or noise measure can be accurately modeled over a large frequency range by a constant value series RC circuit. Then, the input matching circuit can be developed logically as follows:

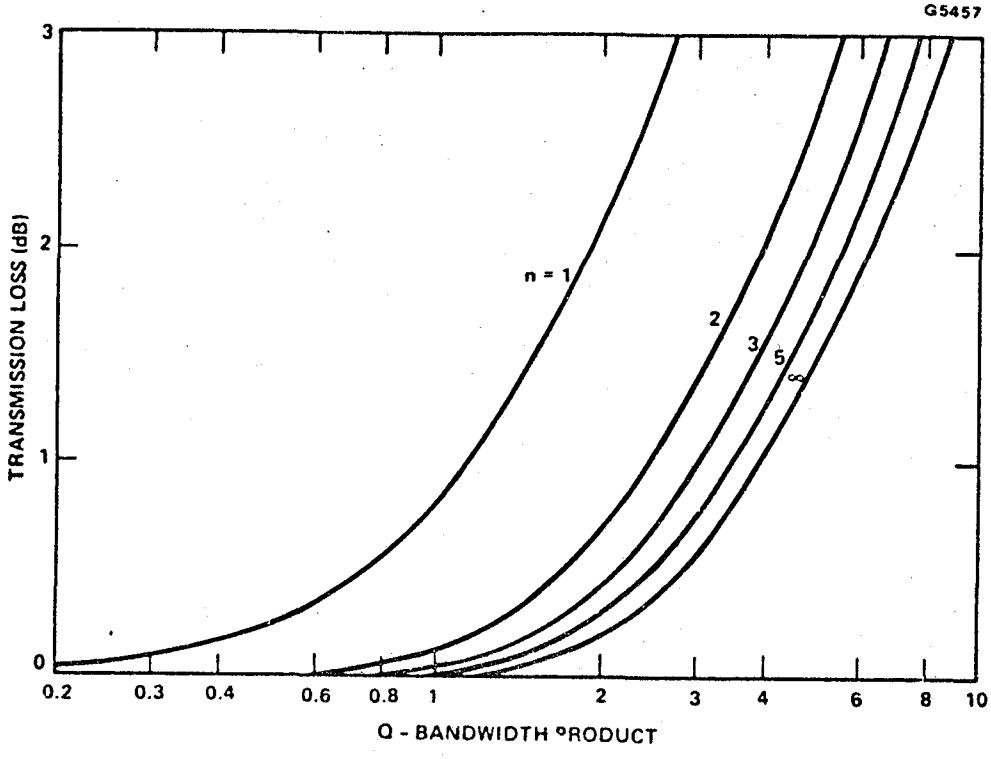


Figure 4-4 Maximum in-band transmission loss as a function of Q-bandwidth product.

1. The required complexity of the matching network is determined while meeting required noise specification. This information is derived from the noise parameters of the device discussed earlier.

2. A network topology is developed and approximate element values are calculated.

3. The network element values are optimized using a computer-aided optimization procedure, such as provided by COMPACT.

When the input matching circuit for the FET chip is matched to minimize noise measure, the device associated gain will have a gain-frequency slope of 5 to 6 dB per octave due to the intrinsic rolloff characteristics of the device. This is the characteristic which would result if the transistor output was conjugately matched at each frequency in the band. To achieve flat gain response over the desired band, the output matching network must compensate for this rolloff. The output network must be designed to provide the necessary impedance matching to achieve the maximum associated gain at the upper end of the desired frequency band. It must also provide a frequency dependent mismatch or resistive attenuation to compensate for the transistor gain slope at lower frequencies. The choice of reactive or resistive compensation is dependent on the application. We chose reactive compensation due to its simplicity.

4.1.2 Low Noise Amplifier

Based on the above procedure, a low noise amplifier circuit was developed. While this circuit was originally developed for our PI-300 device, the same basic circuit was used in all of the fabricated amplifiers by adjusting the circuit element values associated with the device-circuit interface and the initial prematching networks.

4.1.2.1 Amplifier Description - Our approach to the amplifier design emphasizes MIC fabrication technology. In the amplifier stage shown in Figure 4-5, fused quartz substrates, 10 mils thick, with Cr-Au metallizations were used to fabricate the matching networks. Parallel plate chip capacitors, fabricated from high dielectric constant ($\epsilon_r \sim 100$) material, were used for dc blocking and RF

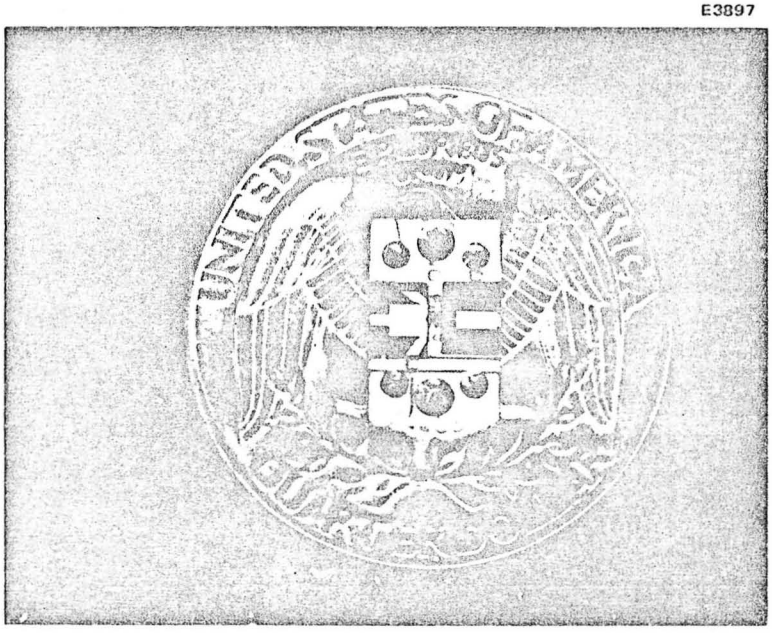


Figure 4-5 Single stage 30 GHz low noise FET amplifier.

bypass. Bond wire 0.7 mil in diameter was used for inductive elements and $\lambda/4$ high impedance transmission lines. The device and circuits are mounted with silver epoxy (Epotek H20E) to an invar carrier plated with nickel and gold. The carrier dimensions are 0.060x0.25x0.390 inches.

The amplifier illustrated in Figure 4-5 utilizes the 0.5x300 μm device. Its equivalent circuit is shown in Figure 4-6a. The amplifiers developed later in the program with different device geometries used the same microstrip circuits, but the prematching circuit was modified to optimize performance. The equivalent circuit for the 0.5x150 and 100 μm devices is shown in Figure 4-6b and that for the 0.25x150 μm devices in Figure 4-6c.

A simulation of the gain performance of an amplifier employing the 0.25x150 μm device is shown in Figure 4-7. The device parameters listed in Section 3.1 were used in this simulation. The input network was designed for a noise match at 30 GHz, while the output network was adjusted to provide gain slope compensation. The initial measured performance of one of the SM08 amplifiers is also shown in the figure for comparison. The agreement with the simulation is fairly good. Return loss measurements indicate that the input and output matching networks were providing minimum return loss just above 30 GHz (31 to 35 GHz); hence the lower gain at 30 GHz.

4.1.2.2 Single Stage Amplifier Results - Each amplifier was evaluated and optimized in a test fixture equipped with dc bias, oscillation suppression networks and waveguide-to-microstrip transitions. Ground walls are mounted on each side of the carrier to raise the cutoff frequency of the guide. A photograph of an assembled tuned amplifier is shown in Figure 4-8. The circuits were tuned by welding gold foil to the circuit or applying silver epoxy. During RF testing, the ends of the transitions are covered by shorting plates.

The waveguide-to-microstrip transition shown in Figure 4-9 is an E-field probe design fabricated on 10 mil thick quartz. The frequency performance from 26.5 to 32.0 GHz of two probes measured back-to-back is shown in Figure 4-10. The insertion loss is typically 0.5 to 0.6 dB over the band, with a return loss of greater than 15 dB over that range.

C-2

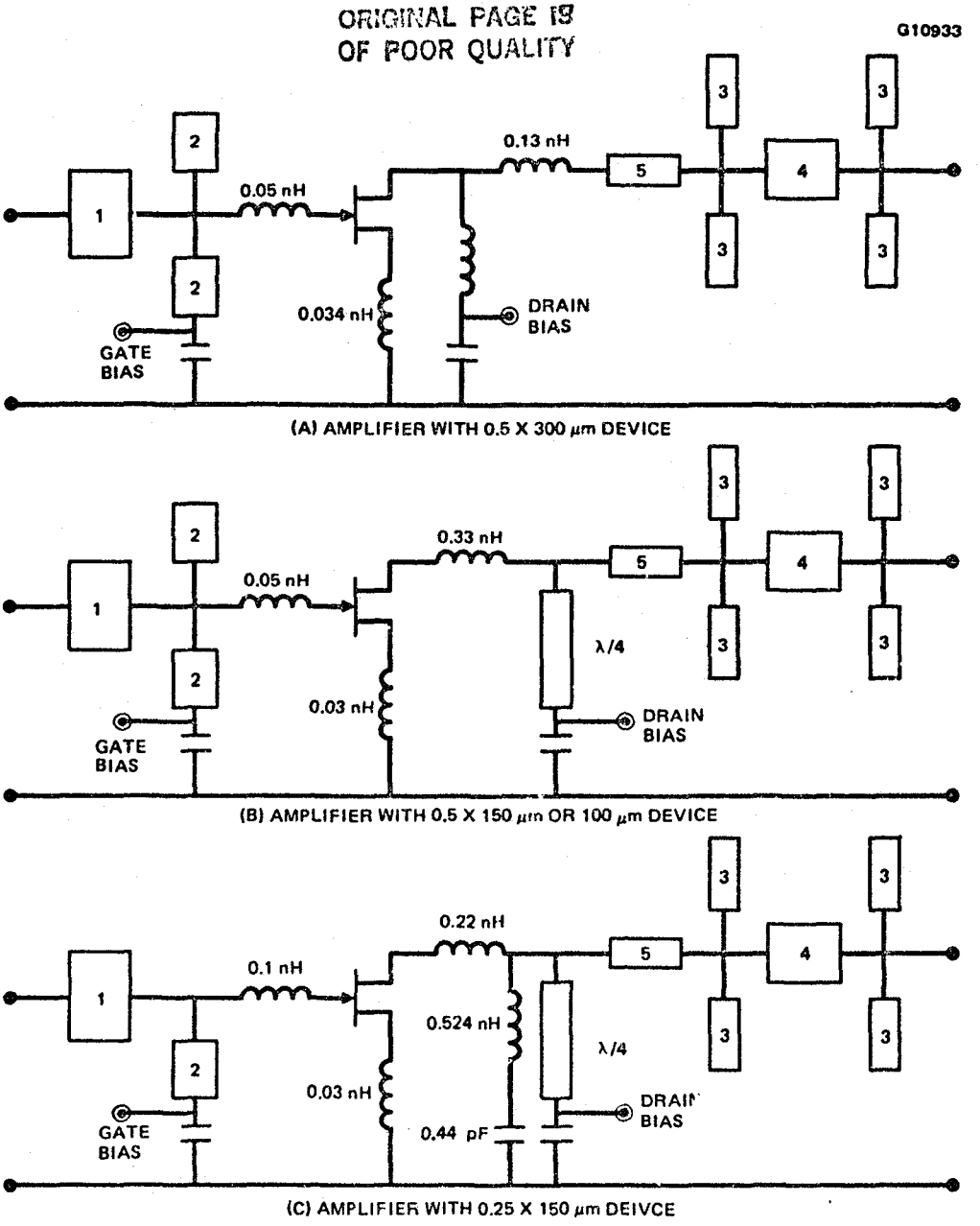


Figure 4-6 Amplifier equivalent circuits.

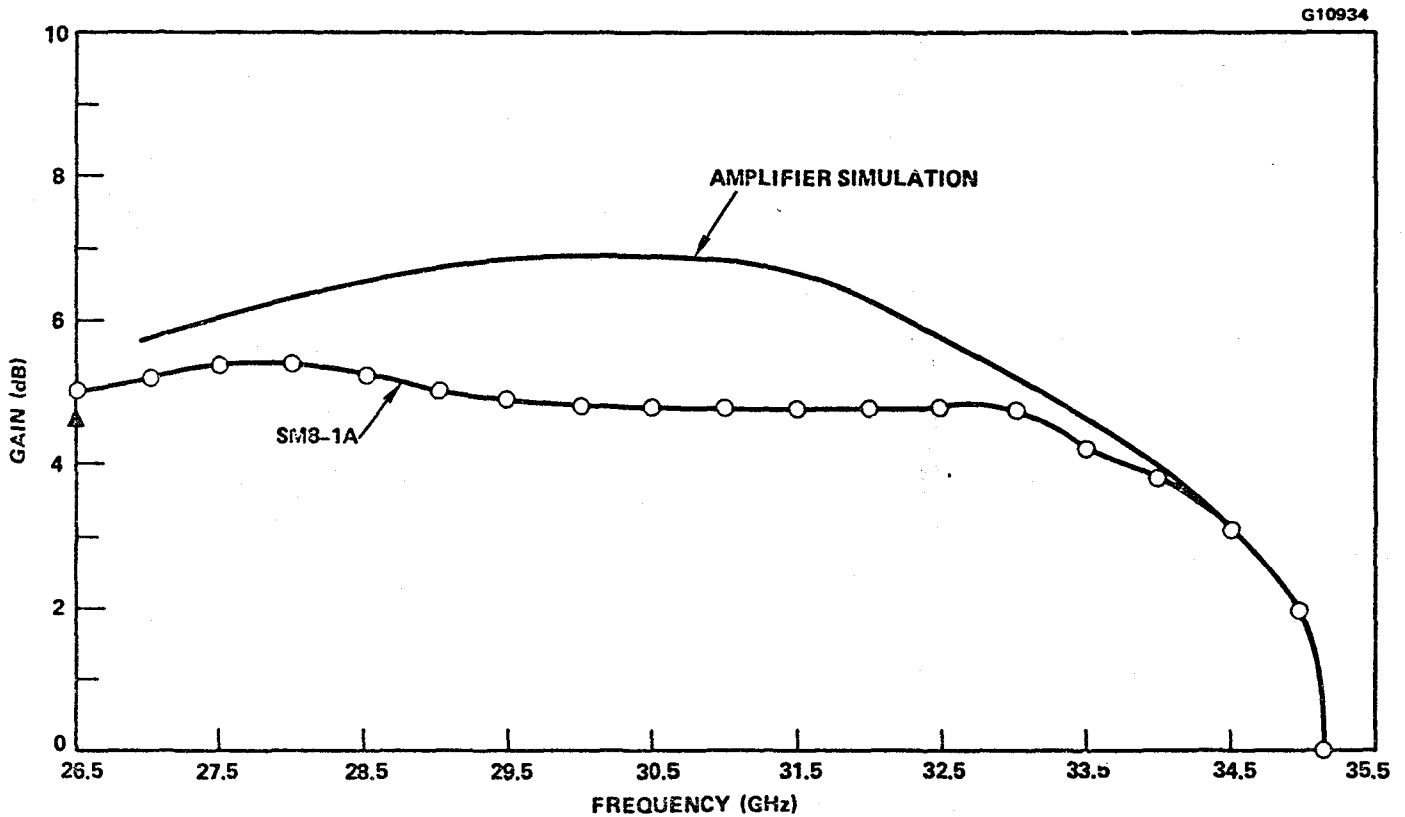


Figure 4-7 Comparison of 30 GHz amplifier simulation and initial measured response for 1/4 μm x 150 μm amplifier.

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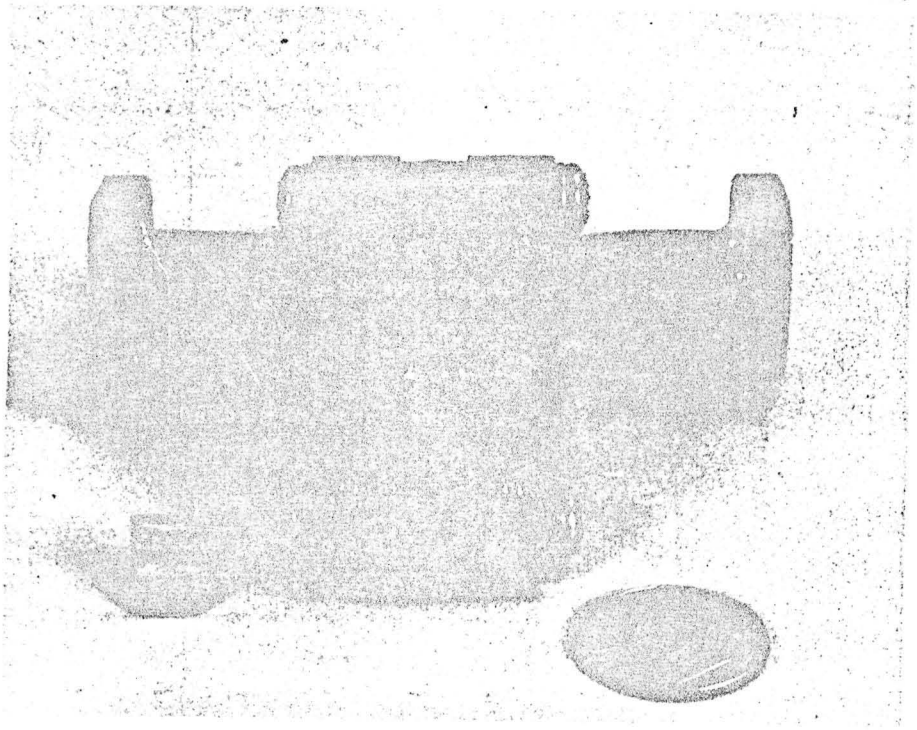

Figure 4-8 Single stage amplifier in test fixture.

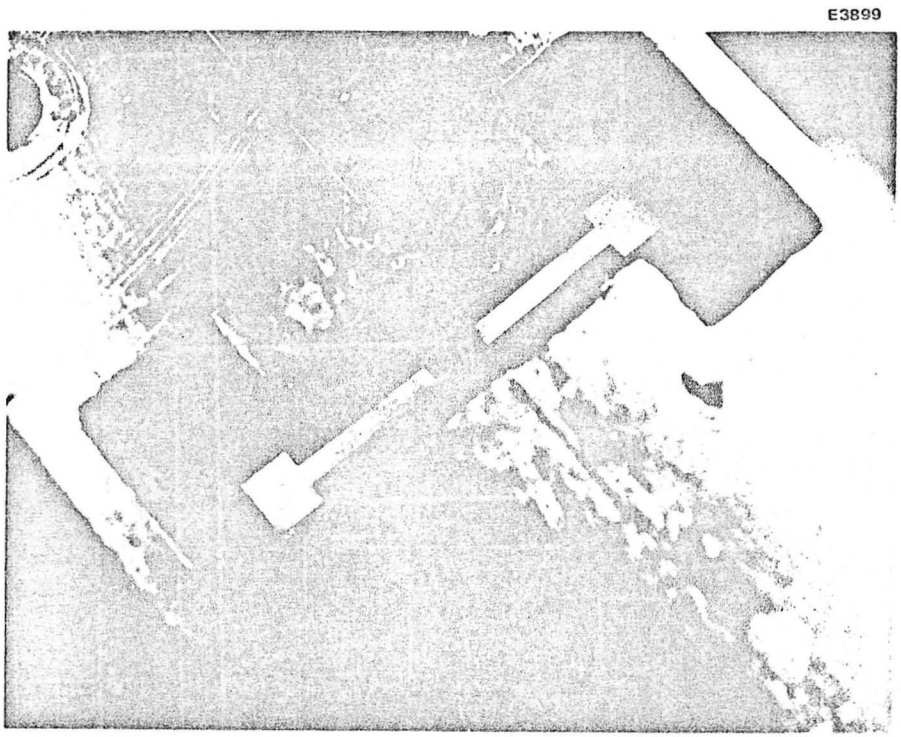

Figure 4-9 Back-to-back Ka-band waveguide-to-microstrip transitions.

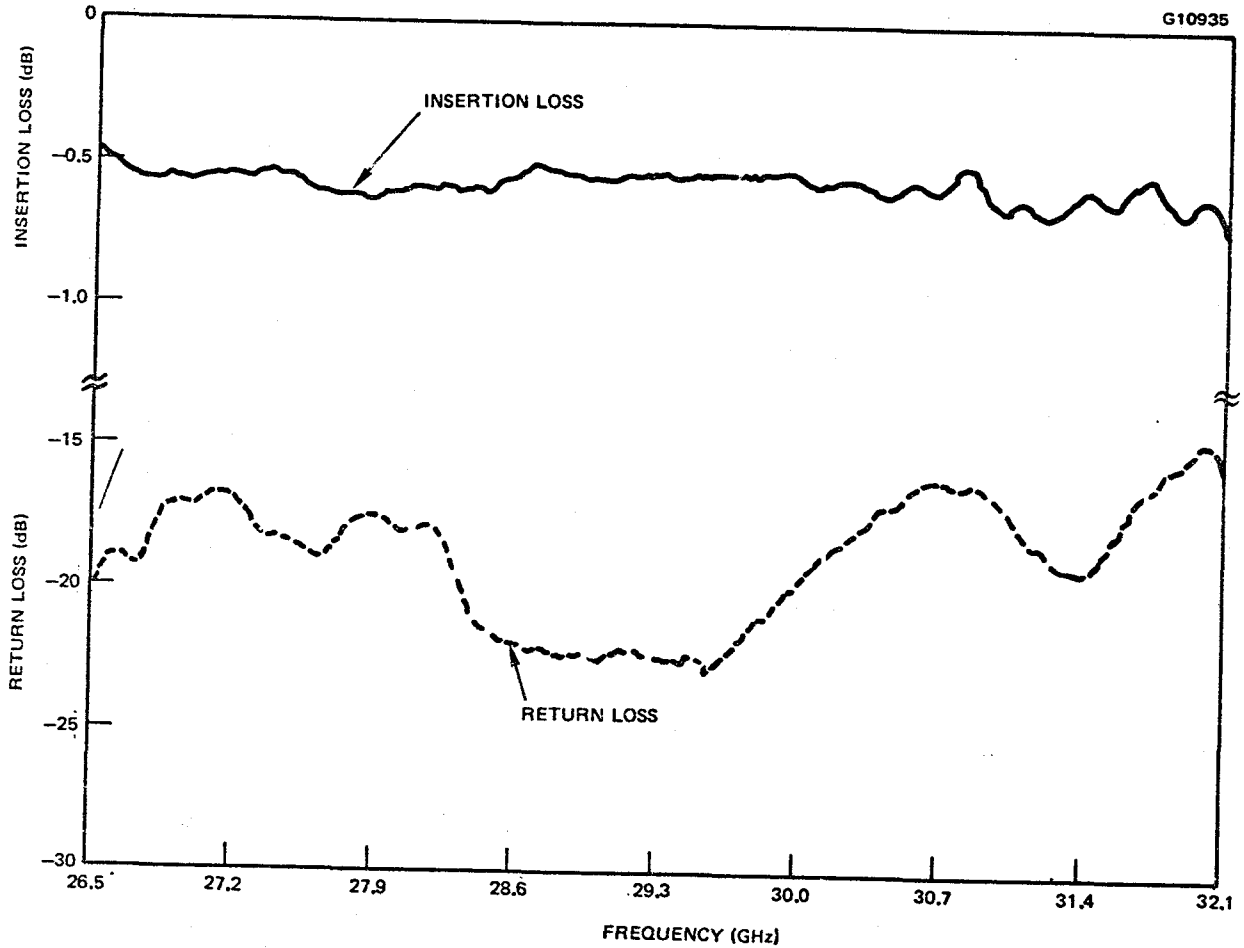

Figure 4-10 Performance of two waveguide-to-microstrip transitions measured back-to-back.

The amplifiers were evaluated and optimized in a swept frequency reflectometer system also capable of measuring noise figure and associated gain. A schematic of the test system is shown in Figure 4-11. When performing swept frequency insertion gain and reflection measurements, the diode detectors are connected to the scalar network analyzer. The system is capable of performing measurements across the band with an accuracy of 0.3 db over a 25 dB dynamic range. For single frequency measurements, the power meters were used.

Spot noise figure measurements can be obtained by resetting the switches without removing the device under test. The noise figure measurement is a double sideband measurement at a 30 MHz IF frequency which is fed into an automatic noise figure meter. The noise source is a calibrated solid state noise source with an ENR nominally of 15.2 dB.

The performance of the single stage amplifiers is summarized in Table 4-1. The data has been corrected for transition loss. A total of eighteen amplifiers were evaluated with the minimum noise figure ranging from 3.6 dB to 6.5 dB at 28.75 GHz. The maximum gain ranged from 5.0 dB to 11.0 dB. The initial amplifier development started with 0.5x300 μm devices from lots L143 and L149. These devices achieved a maximum gain of typically 5.0 to 6.0 dB with one of the L143 devices demonstrating a maximum gain of 11.0 dB at 28.75 GHz. The frequency response of a high gain L149 amplifier (#6) is shown in Figure 4-12. It achieved 8.0 $\pm$ 0.5 dB over a 11.5 percent 1-dB bandwidth. Typically, these devices had relatively poor noise figures and demonstrated RF instability. The 1 dB gain compression point occurred at a power output of +10 dBm for these devices.

The best noise figure achieved with a 0.5 μm gate length device was demonstrated by amplifier #7 fabricated with devices from lot 401. It demonstrated a 3.6 dB noise figure with 3.5 dB associated gain at 28.75 GHz, and achieved a maximum gain of 5.0 $\pm$ 0.5 dB with a 1-dB bandwidth of 4.5 GHz. The output power at the 1 dB gain compression point was +11.0 dBm.

The highest gain wide bandwidth single stage amplifier (#12) employed a 0.5x75 μm SM01 "H" device. This amplifier achieved 9.3 dB gain at 29 GHz.

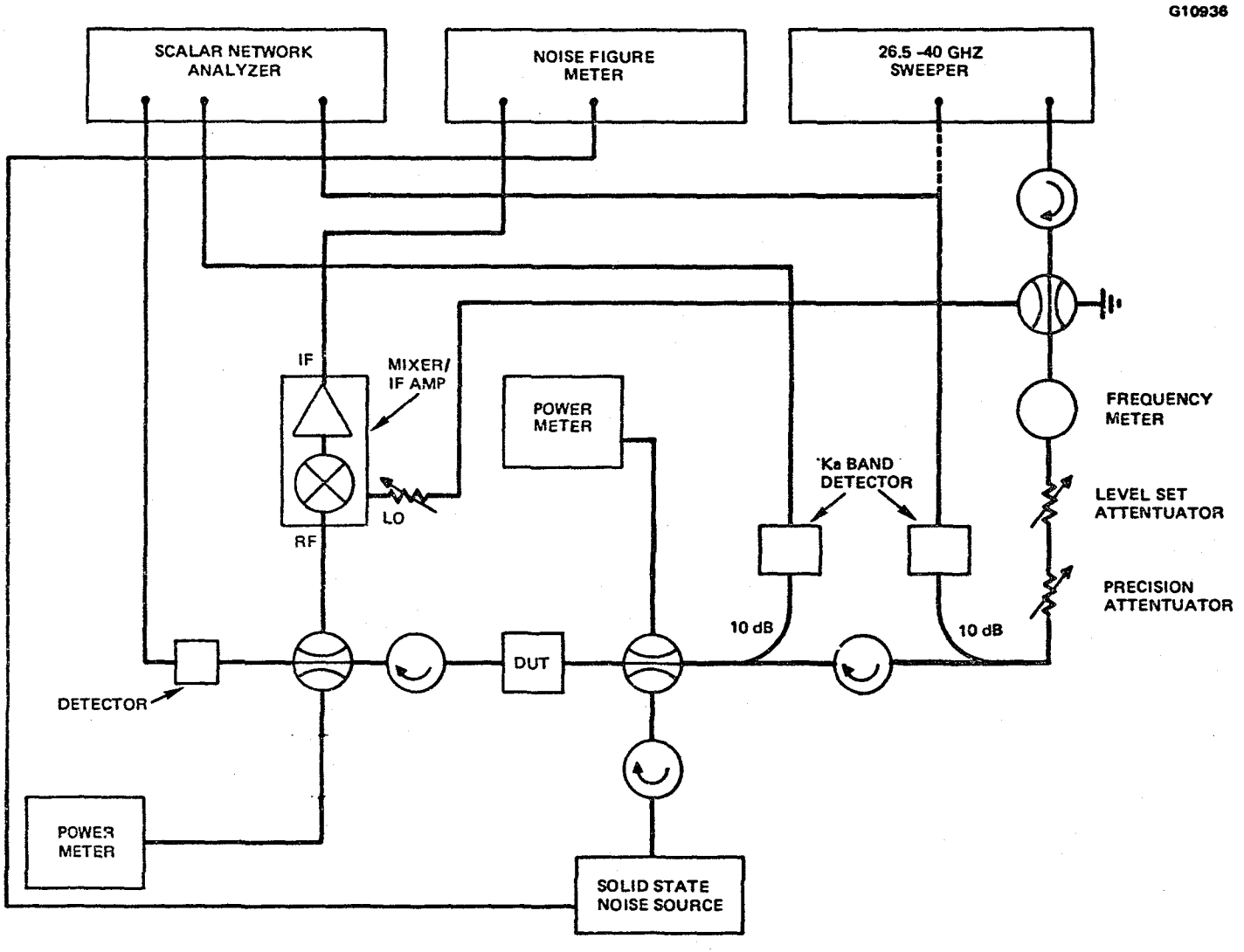

Figure 4-11 Schematic of Ka-band test system.

TABLE 4-1

SINGLE STAGE LOW NOISE AMPLIFIERS

Amplifier #	Device Lot	Device Size (μm)	Maximum Gain		Noise Figure		Output Power @ 1 dB Compression Pt. (dBm)*
			Gain (dB)	1 dB Bandwidth (GHz)	Minimum NF* /Associated Gain (dB)	1 dB Bandwidth (GHz)	
1	L143	0.5x300	6.0 ± 0.25	3.0	----	----	+10.0
2	L143	0.5x300	11.0 @ 28.25 GHz	----	----	----	----
3	L149	0.5x300	6.0 @ 29.5 GHz	----	----	----	----
4	L149	0.5x300	5.0 ± 0.5	3.75	----	----	----
5	L149	0.5x300	6.0 ± 0.5	1.5	----	----	+10.0**
6	L149	0.5x300	8.0 ± 0.5	3.25	----	----	----
7	401	0.5x150	5.0 ± 0.5	4.5	3.6/3.5	1.0	+11.0
8	1429	0.5x150	6.0 ± 0.5	3.25	5.7/3.5	----	----
9	1429	0.5x150	6.5 ± 0.25	3.5	4.4/4.2	2.5	----
10	1429	0.5x150	7.5 ± 0.5	3.5	----	----	----
11	1429	0.5x150	7.0 ± 0.5	3.8	5.0/4.5	3.5	+7.3
12	SM01	0.5x75	8.0 ± 1	4.5	6.5/4.4	----	----
13	SM01	0.5x75	7.0 ± 0.5	5.25	5.1/5.1	3.5	----
14	SM02	0.5x75	6.5 ± 0.5	4.0	4.6/5.7	3.0	----

*@ 28.75 GHz
**@ 30.00 GHz

TABLE 4-1

SINGLE STAGE LOW NOISE AMPLIFIERS (CONTINUED)

Amplifier #	Device Lot	Device Size (μm)	Maximum Gain		Noise Figure		Output Power @ 1 dB Compression Pt. (dBm)*
			Gain (dB)	1 dB Bandwidth (GHz)	Minimum NF* /Associated Gain (dB)	1 dB Bandwidth (GHz)	
15	F2	0.5x100	7.5 ± 0.5	4.5	4.8/5.7	4.5	----
16	F2	0.5x100	6.0 ± 0.5	7.0	4.7/4.6	4.0	----
17	SM08	0.25x150	7.5 ± 0.5	7.85	3.76/6.65	3	----
18	SM08	0.25x150	5.5 ± 2.5	4.5	3.9/5.2	3.5	----

*@ 28.75 GHz

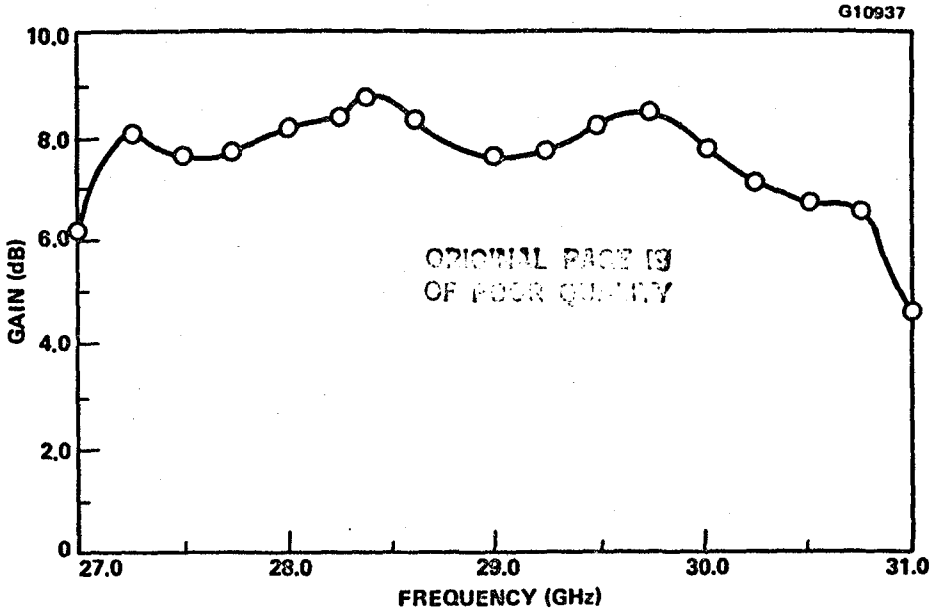

Figure 4-12 Frequency response of amplifier #6.

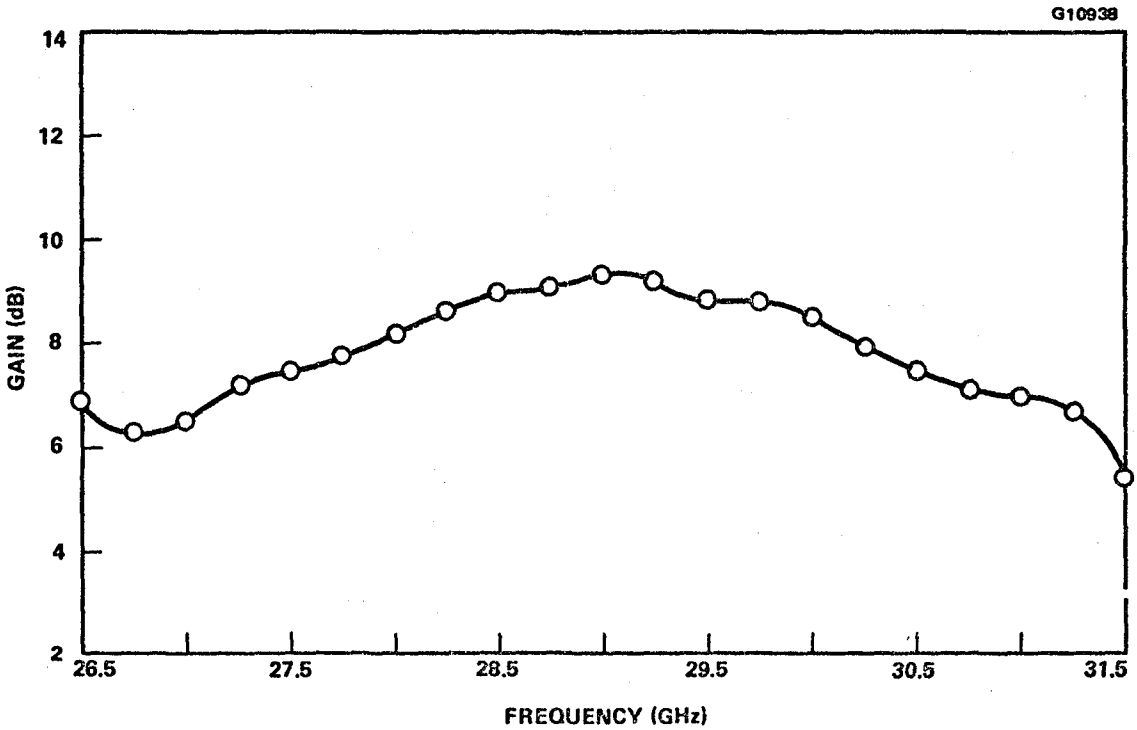

Figure 4-13 Frequency response of the single stage amplifier #12.

The frequency response of this amplifier is shown in Figure 4-13. It also had the highest noise figure; 6.5 dB with 4.4 dB associated gain at 28.75 GHz.

The frequency response of the widest bandwidth amplifier (#16) is shown in Figure 4-14. This amplifier has a gain of 6.0 $\pm$ 0.5 dB over a 23 percent bandwidth. No attempt was made to measure the gain below 26.5 GHz. The noise figure of this stage was 4.7 dB at 28.75 GHz with an associated gain of 4.6 dB.

The widest 1-dB noise bandwidth, 4.5 GHz, was achieved by amplifier #15, whose noise figure and associated gain versus frequency are shown in Figure 4-15. The minimum noise figure is 4.8 dB with 5.7 dB associated gain. The gain varies by 2 dB over this frequency range. Biased for maximum gain, this amplifier produced a gain of 7.5 $\pm$ 0.5 dB over a 4.5 GHz frequency range.

The frequency response of the best single stage amplifier (#17) is shown in Figure 4-16. This amplifier employed our newly developed 0.25x150 µm device from lot SM08. A minimum noise figure of 3.76 dB with 6.65 dB associated gain was achieved at band center frequency, 28.75 GHz. The 1-dB noise bandwidth is 3.0 GHz. Biased for gain, this amplifier achieved a gain of 7.5 $\pm$ 0.5 dB over a 14 percent bandwidth.

The performance of the above amplifier essentially meets the program design goals, 3.5 dB noise figure with 6.0 dB associated gain. However, the effects of the noise figure and associated gain of the stages can be best illustrated by examining the noise measure these stages would achieve. An infinite cascade of identical stages would produce a system noise figure defined as the noise measure (M) of the constituent stages. Used as the front end of a receiver, this noise measure would be the noise figure the receiver would achieve. These differences are illustrated in Figure 4-17, which shows the amplifier noise measure dependence on the individual stage gain and noise figure. Our amplifier results at 28.75 GHz are plotted on this graph. Two of the amplifiers could be cascaded to obtain a noise measure below 5 dB. These are the two amplifiers employing 0.25 µm devices. The best 0.5 µm device amplifier would result in a noise measure near 5 dB. The majority of the 0.5 µm gate length stages would yield an overall receiver noise figure from 5.5 to 6.5 dB.

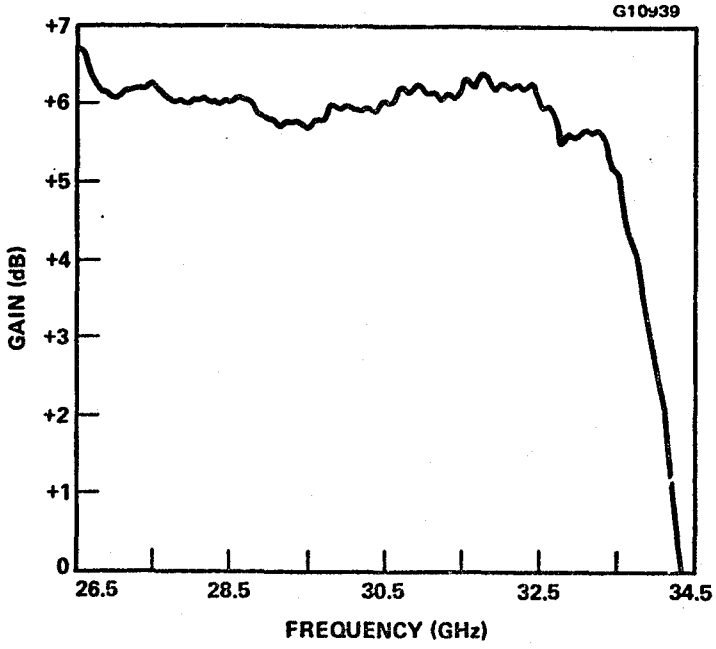

Figure 4-14 Frequency response of amplifier #16.

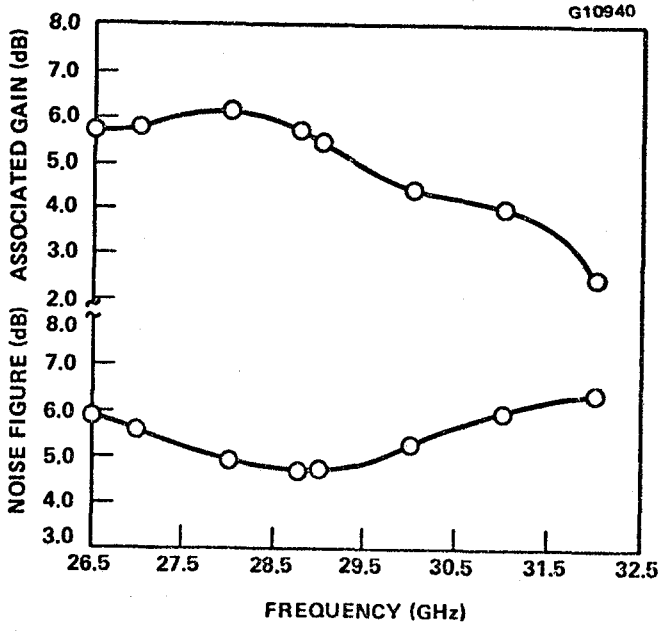

Figure 4-15 Performance of amplifier #15 with the widest 1 dB noise bandwidth.

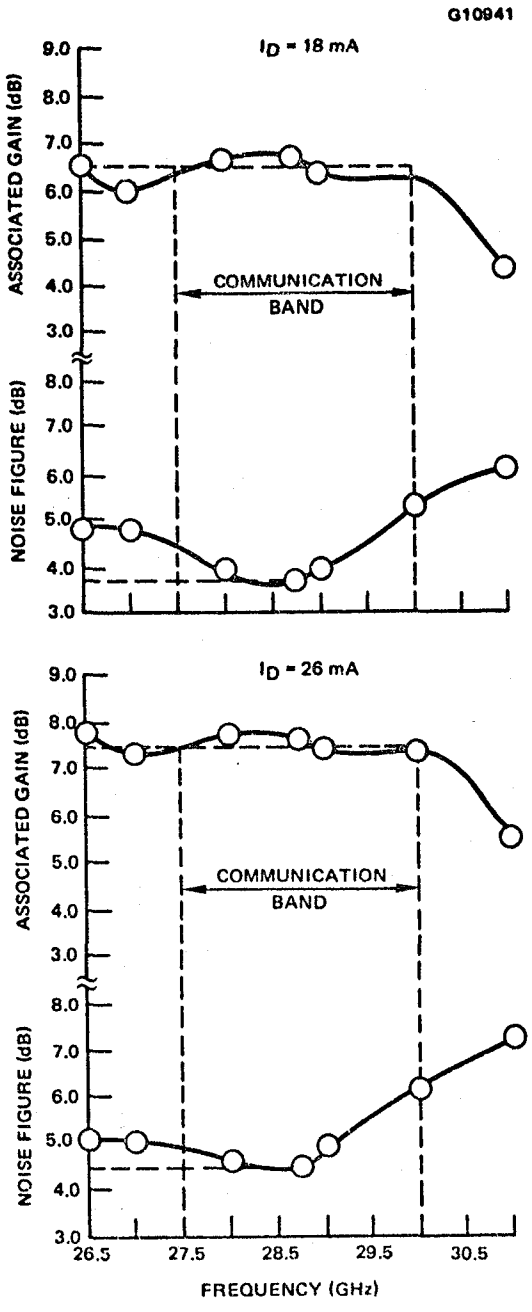

Figure 4-16 Frequency performance of the best single stage amplifier (#17).

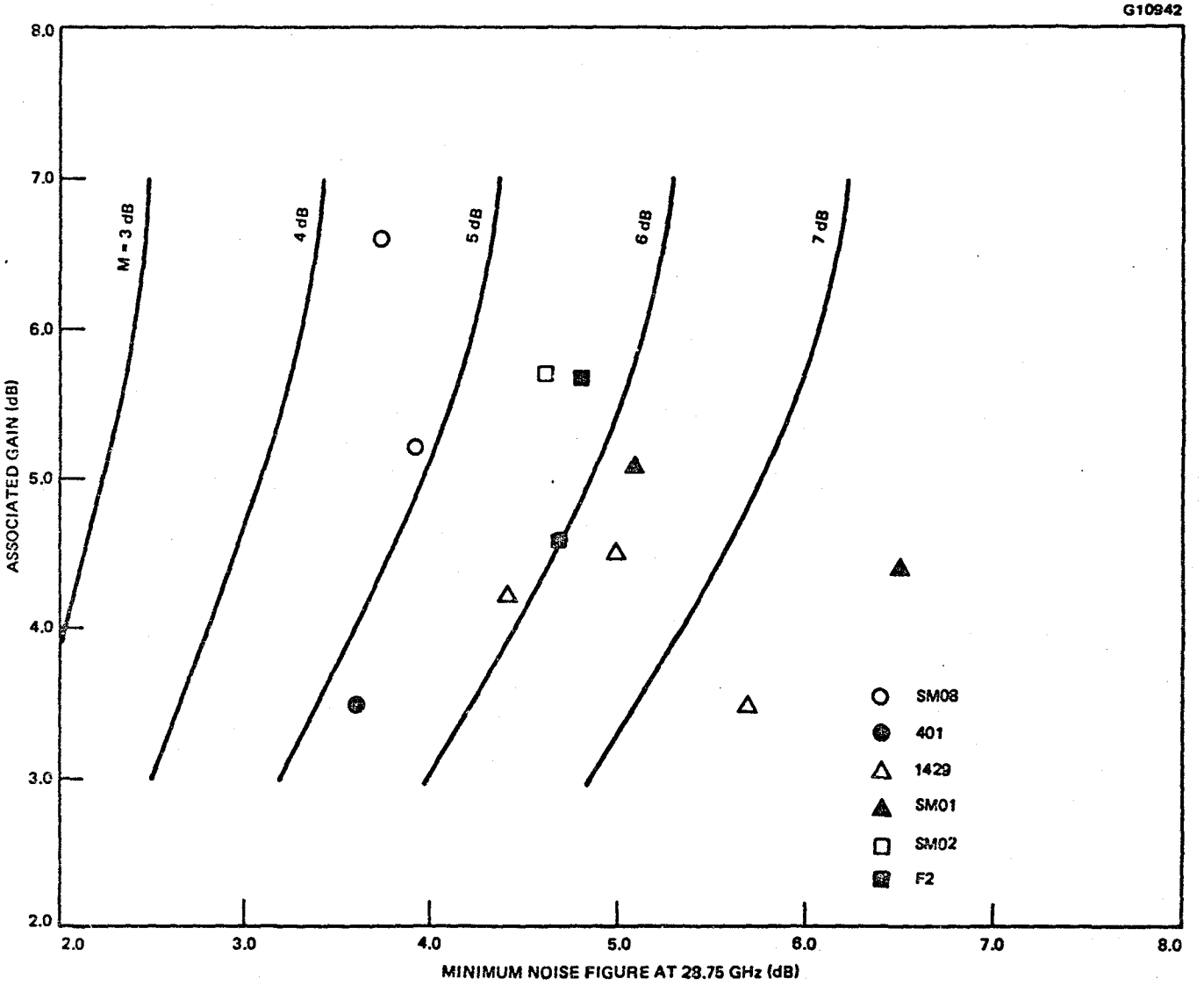

Figure 4-17 Constant noise measure (M) contours for different stage noise characteristics.

4.1.2.3 Multistage Amplifier Results - Using these single stage amplifiers, three multistage units were constructed. Blocking capacitors were added between stages and the units were directly cascaded. The performance of these LNAs are summarized in Table 4-2. The performance of the first two stage amplifier is shown in Figure 4-18 for two bias conditions - minimum noise and maximum gain. Employing devices from lots 401 and 1429, this amplifier demonstrated a maximum gain of 10.8 dB at band center. Its minimum noise figure was 5.8 dB with 7.56 dB associated gain. The stages were successfully cascaded without retuning.

The frequency performance of the second two stage amplifier is shown in Figure 4-19. Biased for maximum gain, this amplifier demonstrated a gain of 11 $\pm$ 0.5 dB from 27.5 to 30.0 GHz. At minimum noise bias, the noise figure was 7.0 dB with 9.4 dB associated gain at 28.75 GHz. A photograph of this two stage amplifier is shown in Figure 4-20.

During the latter part of the program, a three stage LNA was constructed using the two SM08 amplifiers and a F2 amplifier. A photograph of the three stage amplifier is shown in Figure 4-21. The frequency response of this LNA at minimum noise figure bias is shown in Figure 4-22. The minimum noise figure is 4.4 dB with 17 dB associated gain at 28.75 GHz. The gain is flat to $\pm$ 0.5 dB over the band from 26.5 to over 30.0 GHz. The frequency response at maximum gain bias is shown in Figure 4-23. The gain, 20.0 $\pm$ 1 dB, extends from 26.5 to 30.5 GHz. The minimum noise figure at band center is 4.8 dB. The gain compression characteristics of this amplifier at 28.75 GHz are shown in Figure 4-24. The output power at the 1-dB gain compression point is +4 dBm, and +5 dBm for the high gain and the minimum noise bias conditions, respectively.

4.1.3 Cryogenic Test

Stable, low power and low cost GaAs FET amplifiers are attractive alternatives to paramps in intermediate performance cryogenically cooled (20°K) microwave receiving systems, when the lowest noise, high cost maser is not required. Cooled FET amplifiers at 5 GHz (20°K)[14] and 23 GHz (77°K)[15] have demonstrated noise temperatures 3 to 5 times lower than 300°K units.

TABLE 4-2

MULTISTAGE LOW NOISE AMPLIFIERS

Amplifier #	Number of Stages	Maximum Gain Bias		Minimum Noise Bias		1 dB Bandwidth (GHz)	Output Power 1 dB Compression Pt. (dBm)*
		Gain (dB)	1 dB Bandwidth (GHz)	NF* (dB)	Associated Gain (dB)		
1	2	10 ± 0.5	2	5.85	7.56	2	----
2	2	11.5 ± 0.5	2.8	7.0	9.4	----	----
3	3	10.0 ± 1	4.2	4.4	17.35	2.15	+4.2

*@ 28.75 GHz

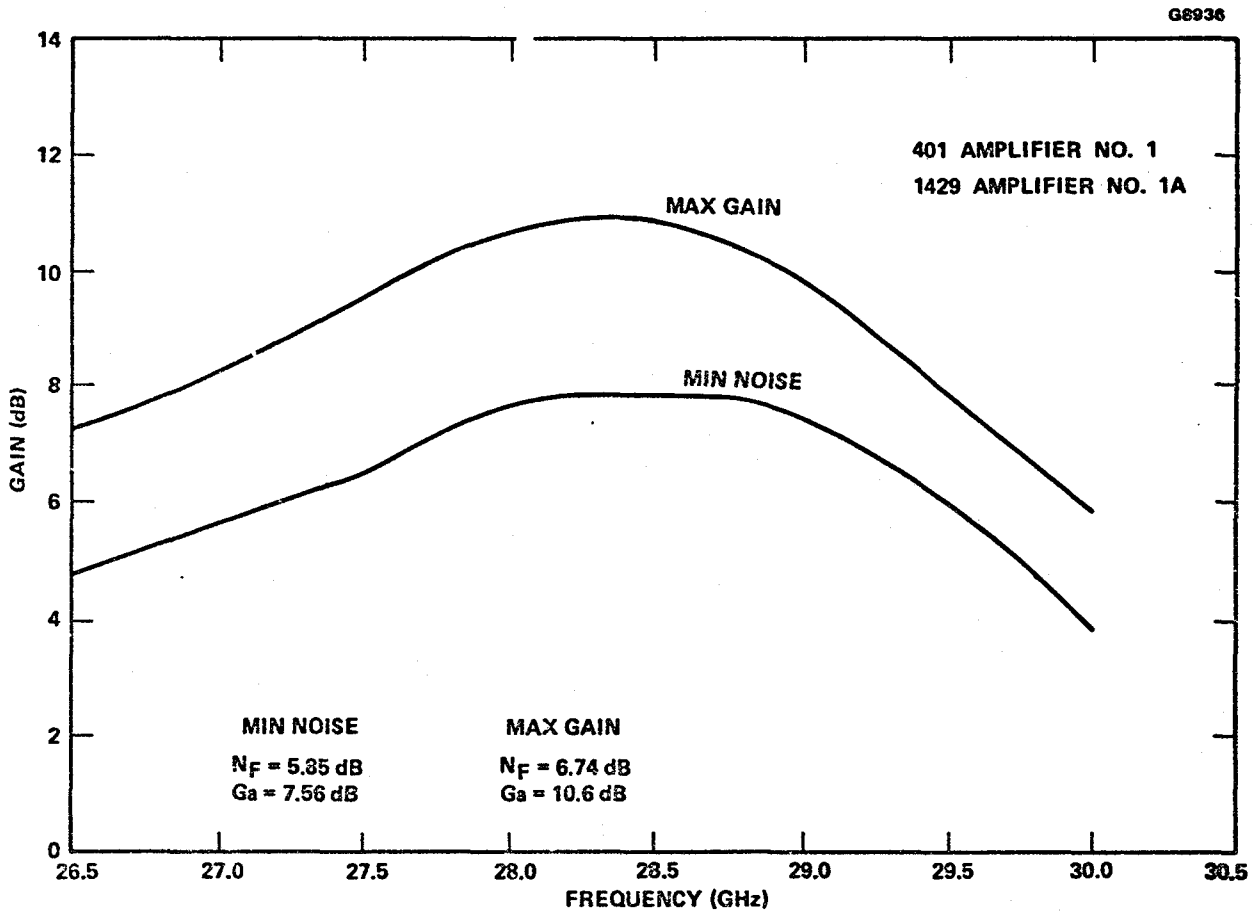

Figure 4-18 Frequency response of two-stage amplifier #1.

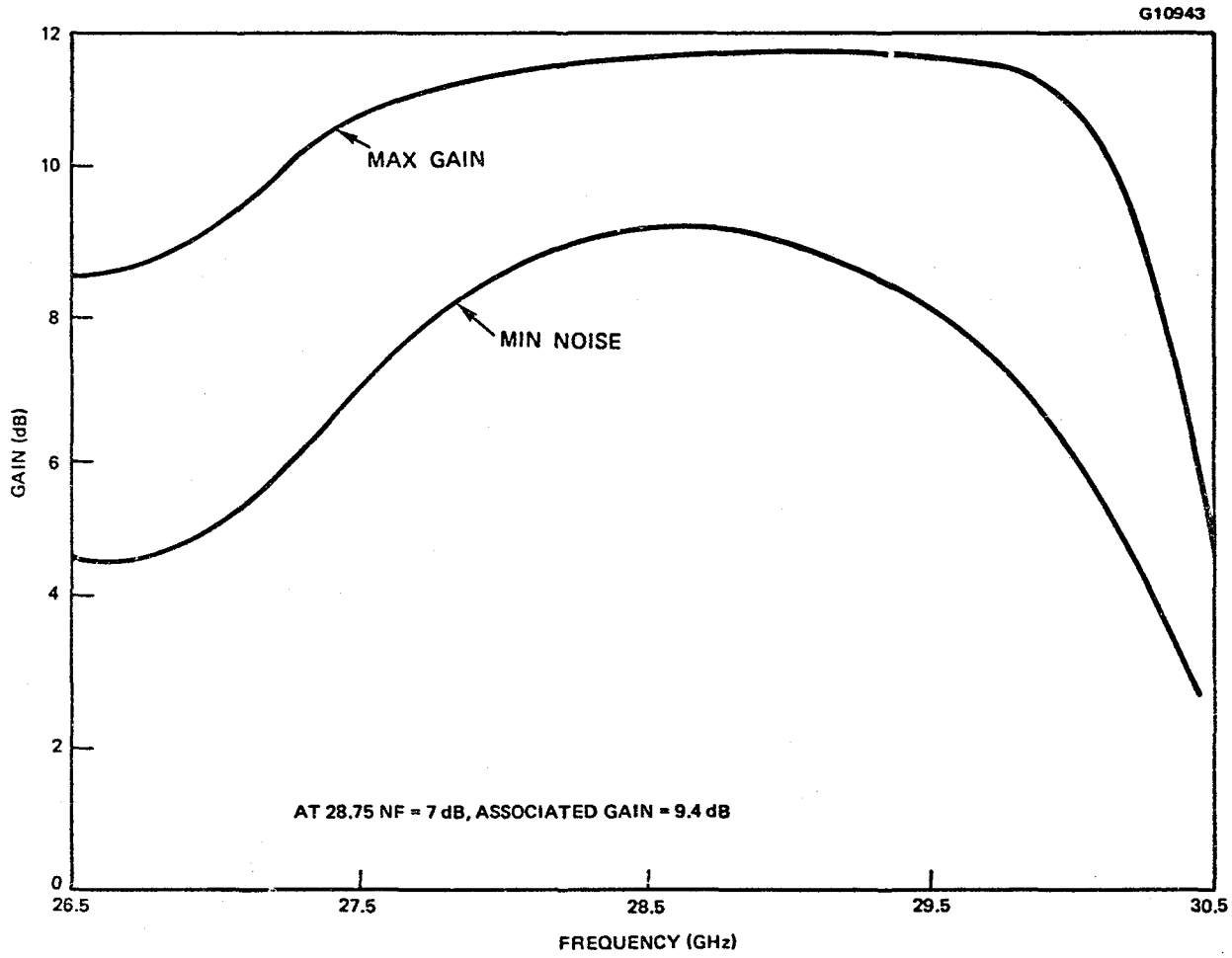

Figure 4-19 Frequency response of two-stage 30 GHz amplifier #2.

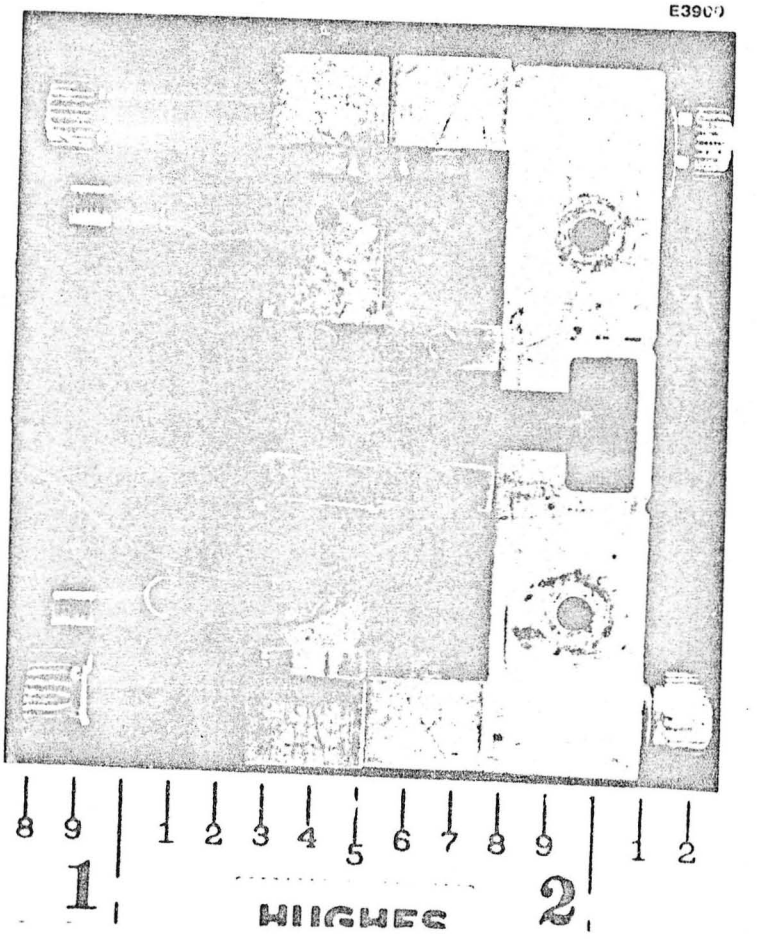

Figure 4-20 Two-stage amplifier #2.

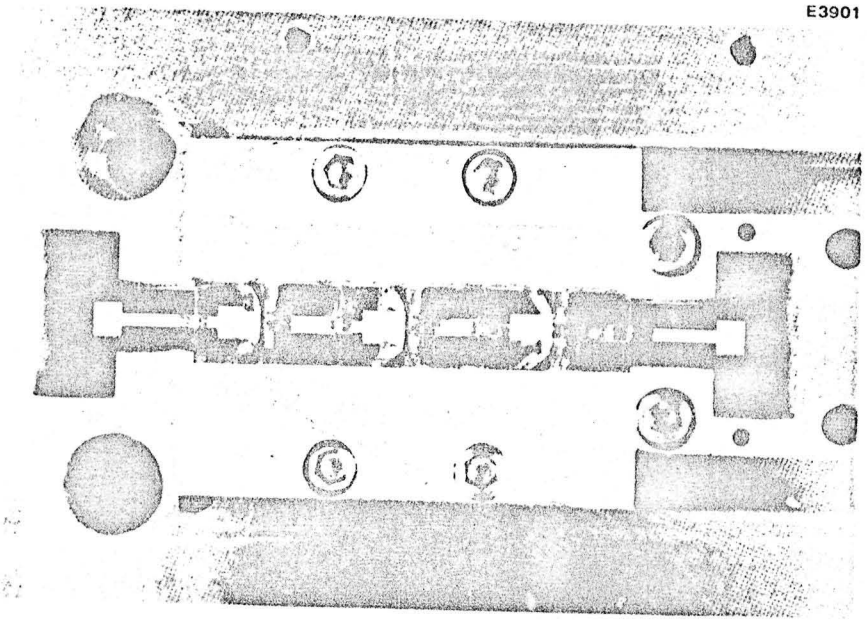

Figure 4-21 Three stage 30 GHz low noise amplifier #3.

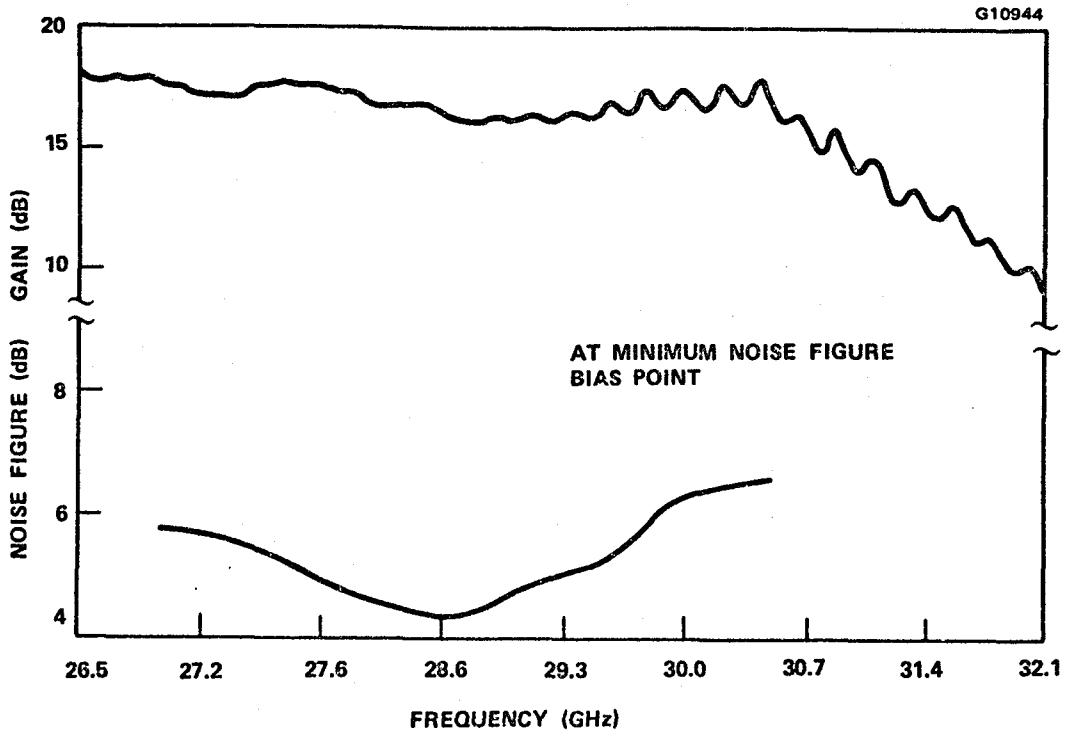

Figure 4-22 Frequency response of three-stage amplifier biased for minimum noise figure.

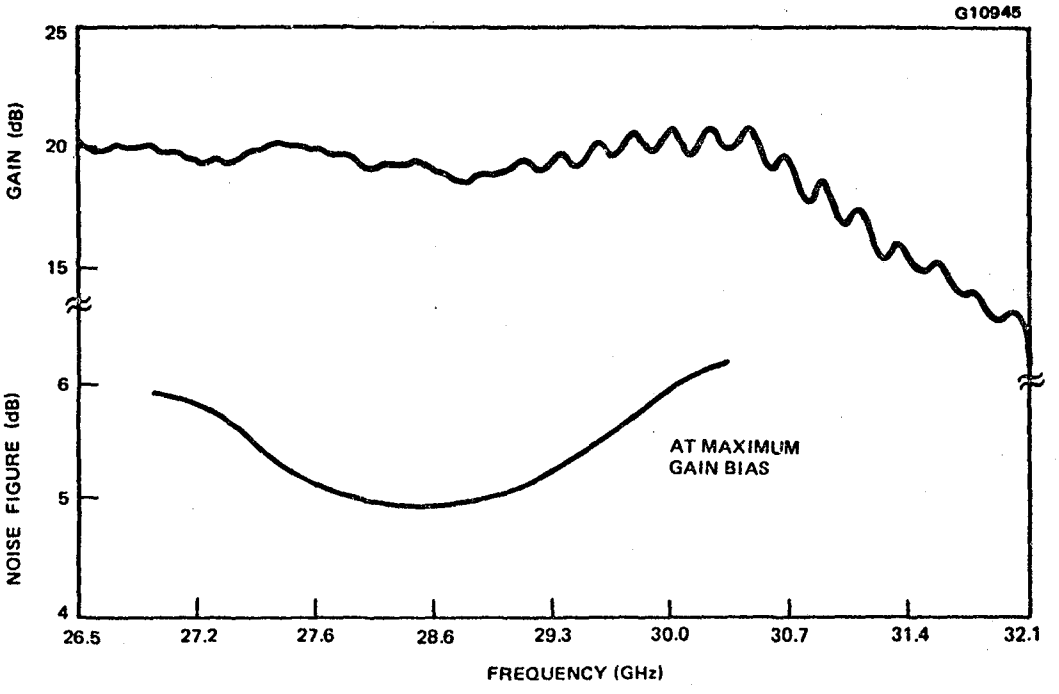

Figure 4-23 Frequency response of three stage amplifier biased for maximum gain.

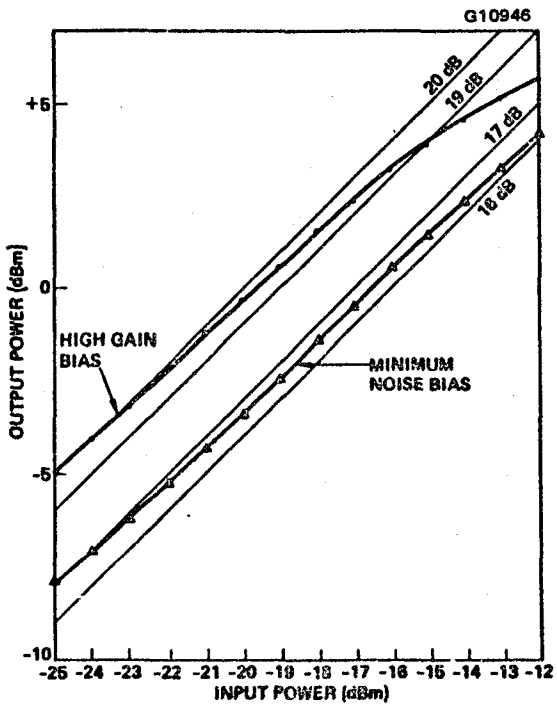

Figure 4-24 Gain compression characteristics of the 3-stage low noise amplifier.

The design of low noise FET amplifiers for cryogenic operation involves a careful study of thermal and electrical properties of the

- Assembly materials (epoxy, solder)
- Substrates and carriers
- Metallization layers (circuits and device connections)
- Device parameters (RF and dc) and
- Circuit elements

to characterize and maximize device cooling and account for device-circuit changes to optimize performance. These experiments represent an initial investigation of our assembly techniques, device-circuit integrity and device RF and dc performance at cryogenic temperatures. Special design and assembly procedures were not implemented on the units evaluated and hence optimum performance improvements at low temperatures were not expected.

4.1.3.1 Amplifier Description - Five Ka-band amplifiers, operational at frequencies ranging from 26.5 to 38.0 GHz at room temperature, were selected for cryogenic evaluation. Basically, two types of amplifiers were chosen. Four of the units were built in the type 1 configuration; two for 30 GHz operation (Figure 4-25a) and two for 40 GHz operation (Figure 4-25b). The device was mounted to a brass carrier between 50 Ω microstrip lines fabricated on 10 mil thick fused quartz substrates with integrated waveguide-to-microstrip transitions. The device, substrates, and chip capacitors were mounted with silver epoxy. The entire matching network consists of the gold wire and ribbon networks surrounding the chip. Approximate equivalent circuits for the amplifiers are shown in Figure 4-26. The FETs were experimental 0.5x75 m, "H" type devices from lots SM02 and SM04. The size of the amplifier is 0.110x0.250 inch. During test the amplifier was mounted in the waveguide test fixture as shown in Figure 4-27. The type 2 amplifier, one of our regular 30-GHz units, has been previously described.

4.1.3.2 Test Description - Cryogenic tests were conducted at the Naval Research Laboratory (NRL) in cooperation with Dr. D.L. Thacker of the E.O. Hulburt Center for Space Research. The tests were performed using their

E3902

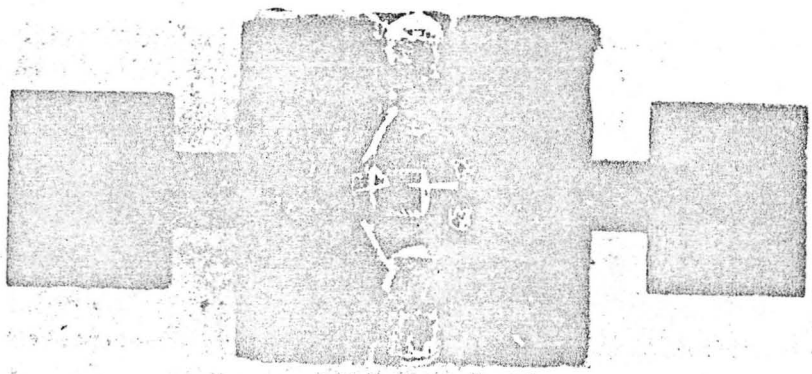

Figure 4-25a 30 GHz type 1 cryogenic amplifier.

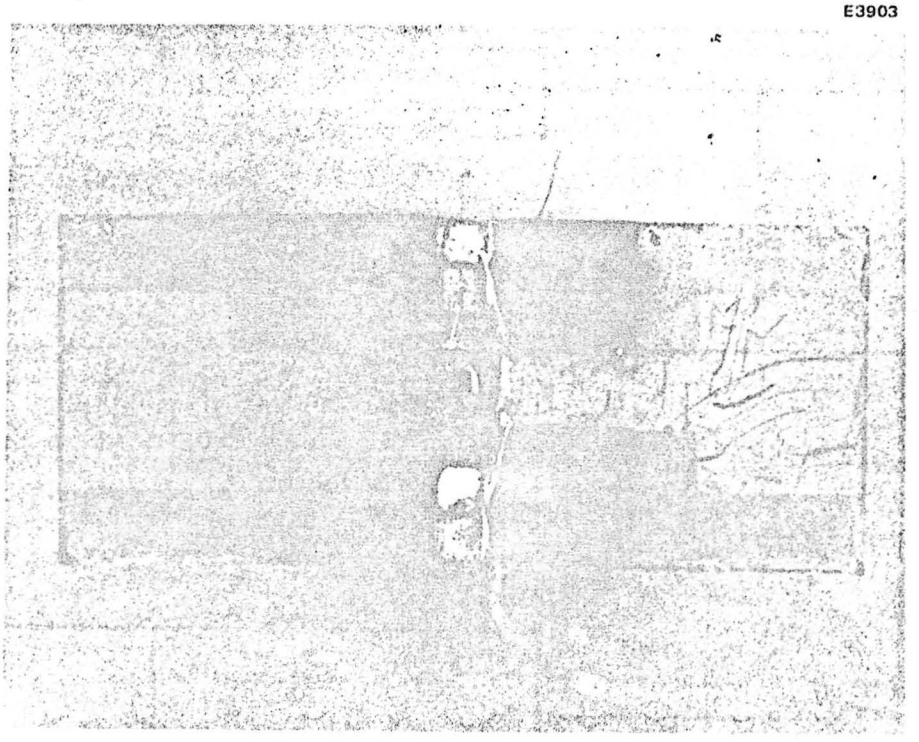

Figure 4-25b 40 GHz type 1 cryogenic amplifier.

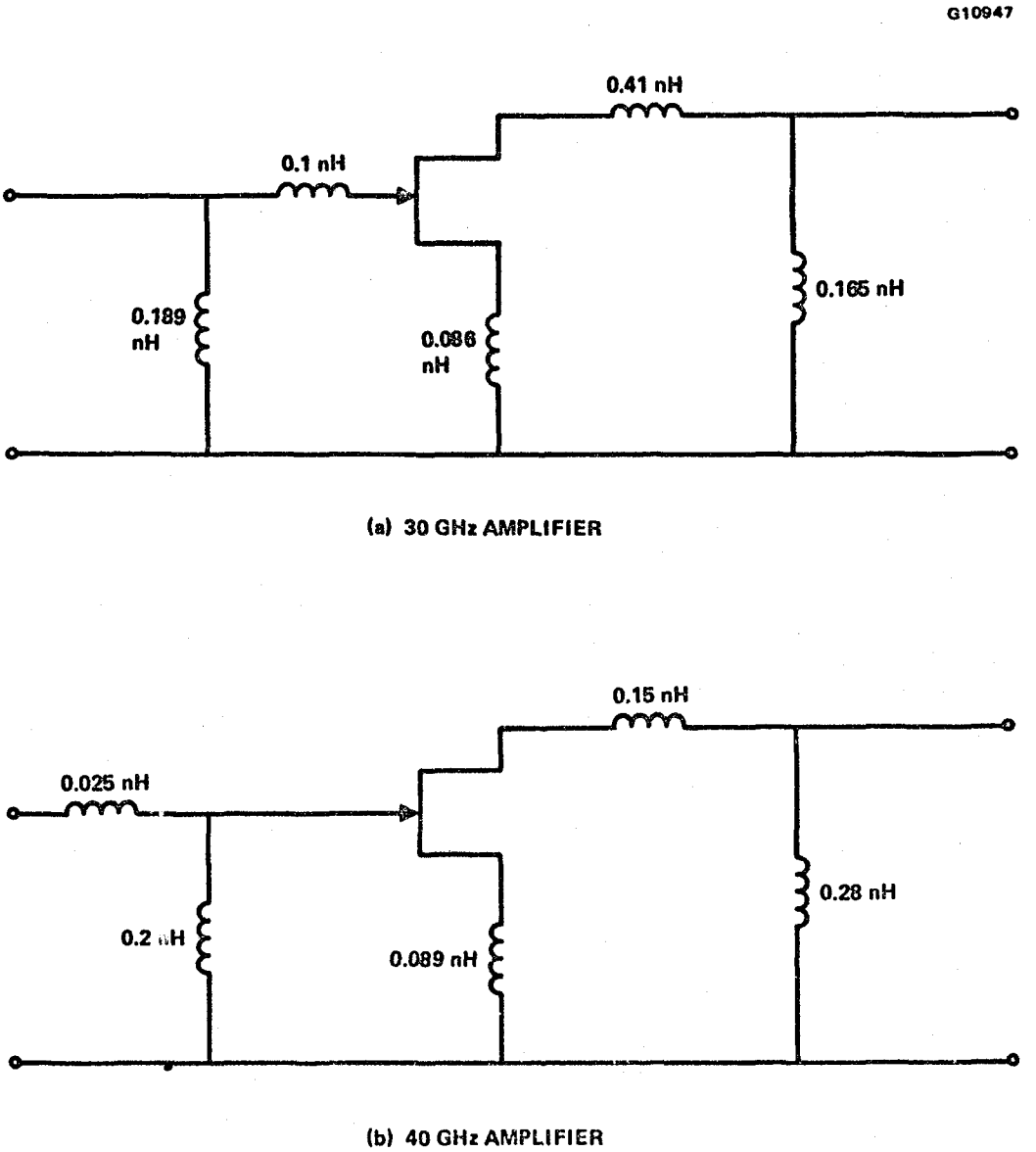

Figure 4-26 Equivalent circuits of type 1 cryogenic amplifiers.

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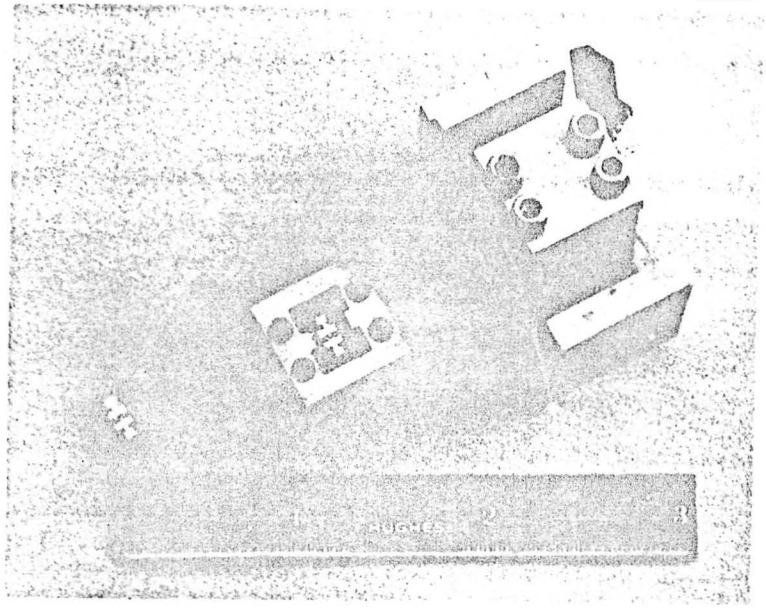

Figure 4-27 Type 1 Ka-band amplifier and test fixture for cryogenic tests.

vacuum evacuated waveguide test system which included a Cryogenic Technology Inc., model 350 refrigerator. Hot (ambient) and cold (77°K) loads were employed in a double sideband Y factor noise test determining both noise temperature and gain.

Noise tests are more complicated at temperatures other than 290°K because assumptions made during room temperature measurements are no longer good approximations. One must determine not only system losses, L, but also their temperature, T_L.

For proper evaluation of the noise temperature of a component imbedded in a system, such as a matched loss, L, cascaded with an amplifier with noise temperature, T_e, the overall noise temperature, T_e' is given by

$$T_e' = (L - 1)\, T_L + LT_e \qquad (4.1\text{-}6)$$

so that, the loss ahead of an amplifier multiplies T_e by L and adds $(L - 1)T_L$ to the overall noise temperature.

A similar expression can be written for loss following an amplifier. This is complicated by the fact that in the cryogenic test the temperature of the loss is not constant throughout the system, as those losses are in the components interfacing with the device under test, and probably have a temperature gradient along their length. The task is further complicated due to time consuming calibrations at both room temperature and 24°K.

The amplifiers were tested individually at room temperature and 24°K. The cooling from 296°K to 24°K occurred over approximately an 8-hour time period due to system constraints and to avoid thermal shock to the components, however warmup times were significantly shorter.

4.1.3.3 Cryogenic Test Results - The five amplifiers were tested and optimized before being taken to NRL for measurement. The initial performance measured at Hughes TRC is listed in Table 4-3 for each unit, and represents the performance level at the test fixture ports. These amplifiers were representative of

TABLE 4-3

PERFORMANCE OF CRYOGENIC TEST UNITS MEASURED AT TRC

Amplifier		Device		Parameter		
#	ID	Lot	Size	Noise Figure (dB)	Associated Gain (dB)	Frequency (GHz)
1	H-0	SM04	0.5x75 μm	6.0	6.2	30
2	H-3	SM02	0.5x75 μm	5.3	6.7	37
3	H-4	SM02	0.5x75 μm	6.1	5.6	38
4	H-5	SM02	0.5x75 μm	5.55	6.2	31
5	A-2	F2	0.5x100 μm	4.7	4.6	28.75*

*corrected for transitions (0.5 dB total)

average performance Ka-band FET amplifiers at the time. Except for amplifier #5, the noise figures of the units were not optimized. The two amplifiers constructed for 30-GHz operation performed best at 30.0 and 31.0 GHz. The 40-GHz units operated best at 37.0 and 38.0 GHz.

The most extensive data was taken on amplifier #5. Room temperature (296°K) and 24°K, gain and noise temperature measurements were taken versus drain current, I_{DS}, at 28.15, 29.0, and 29.95 GHz and are presented in Figure 4-28a,b,c for each frequency. The data represent performance at the test fixture ports without retuning to cryogenic temperatures. The noise temperature minimum is 2.2 to 3.3 times lower at 24°K than at 296°K depending on the frequency. At higher drain currents the degree of improvement increases, ranging from 2.7 to 4.5. At two frequencies the associated gain increased at 24°K as expected. The reason for the decrease in gain at 29.0 GHz has not been determined at this time, but is probably due to circuit detuning effects.

Improvements in noise temperature by factors of 3 to 5 have been reported with our results falling below that range. This may be an indication that:

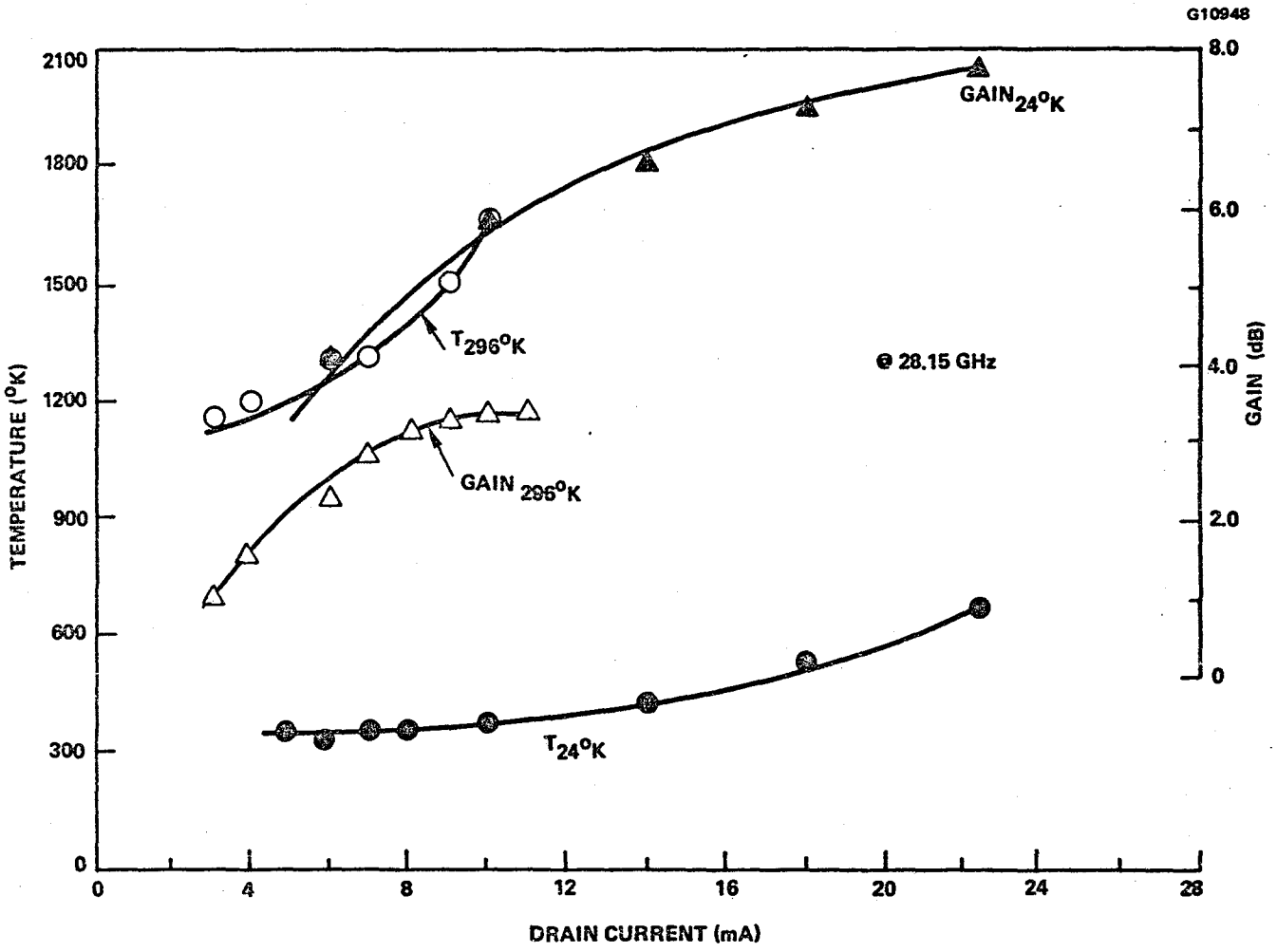

Figure 4-28a Performance of amplifier #5 at 296°K and 24°K at 28.15 GHz.

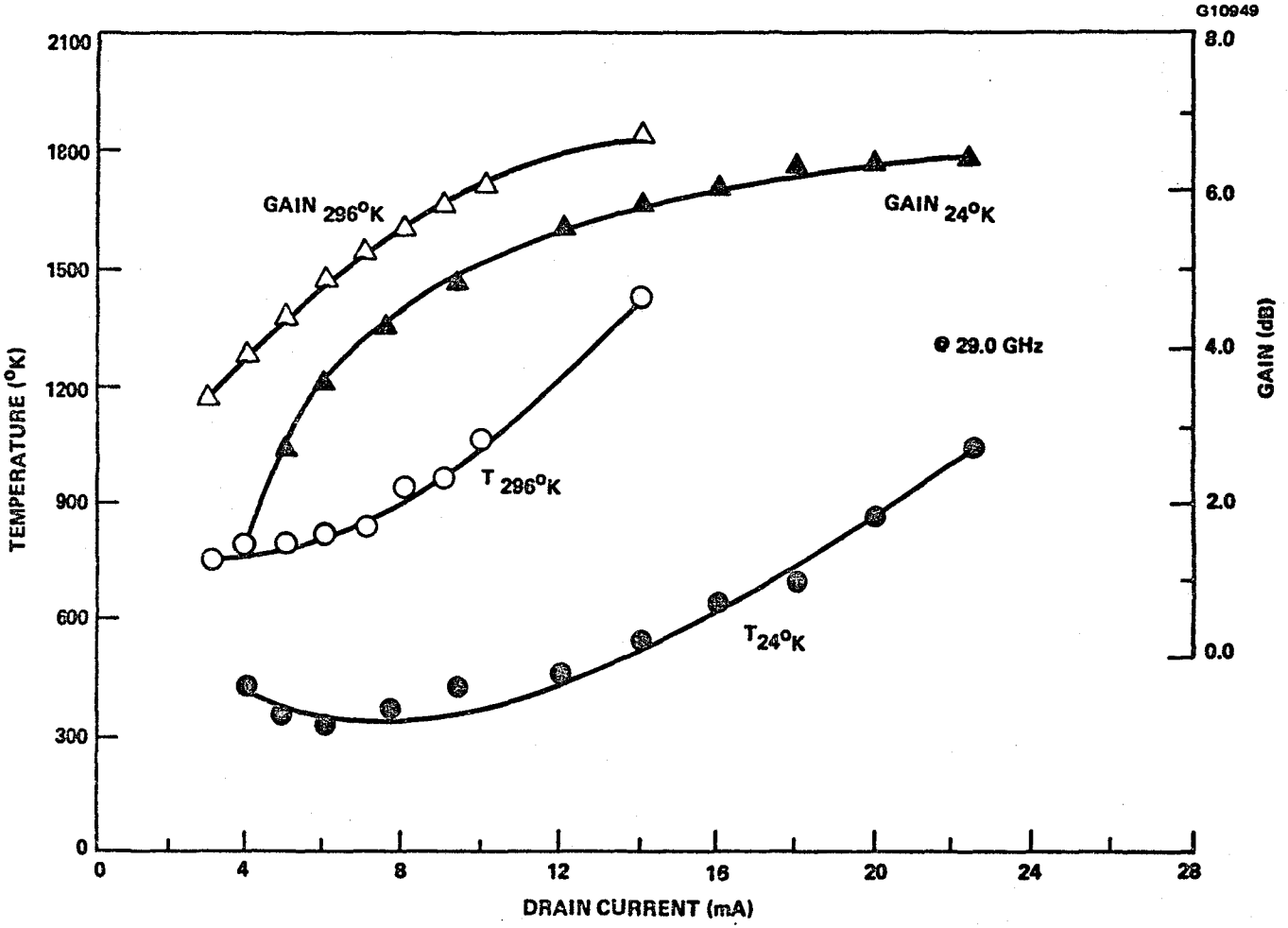

Figure 4-28b Performance of amplifier #5 at 296°K and 24°K at 29.0 GHz.

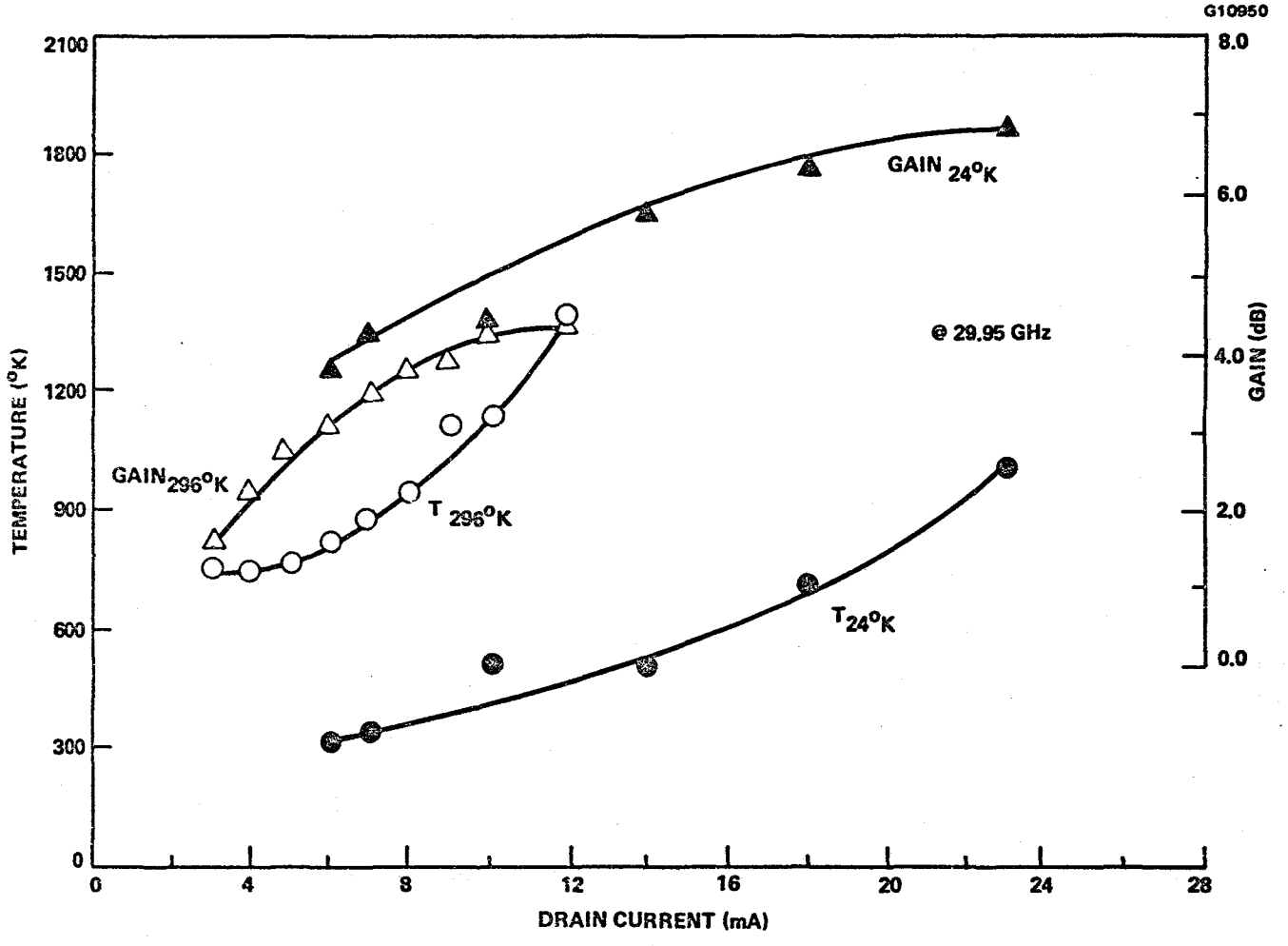

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Figure 4-28c Performance of amplifier #5 at 296°K and 24°K at 29.95 GHz.

- Nonoptimum noise match at the cryogenic temperatures.
- Our devices have a higher ratio of nonthermal to thermal noise than other devices due to geometry or materials.
- The device channel was not optimally cooled due to a high thermal resistance, possibly caused by the silver loaded epoxy used to mount the device and circuits.

Additionally, the thermal path provided by the 0.7 mil bond wire on the source and drain of the devices may have significantly reduced the heat flow from the device.

One interesting aspect of the results is shown in Figure 4-29. When cooled, the minimum noise temperature is approximately the same for all frequencies despite the differences at 296°K.

Variations in device dc parameters with temperature can be used to determine the variation with temperature of material parameters important in noise theory, mobility and saturation velocity for example. Insufficient data prevents any definite conclusions, however the saturated drain current, I_{DS} and gate voltage were measured. The drain current, I_{DS}, versus gate source voltage, V_{GS}, at 3.0 volts drain-source, V_{DS}, is shown in Figure 4-30 for the device operating at 296°K and 24°K. I_{DS} is 4 to 6 mA higher at 24°K than at 296°K for any gate voltage. The slope of the curve represents the transconductance, however, this is not the true device transconductance g_m, which is given by

$$g_m = g_m' / (1 - g_m' R_s) \qquad (4.1\text{-}7)$$

where g_m' is the measured external value and R_s is the source resistance. If we assumed R_s was constant, then the device transconductance, g_m, increased by greater than 28 percent when cooled to 24°K. Additionally, if we assumed at 3 mA the device is pinched off, the pinchoff voltage, V_p, increased by 33 percent going from hot to cold.

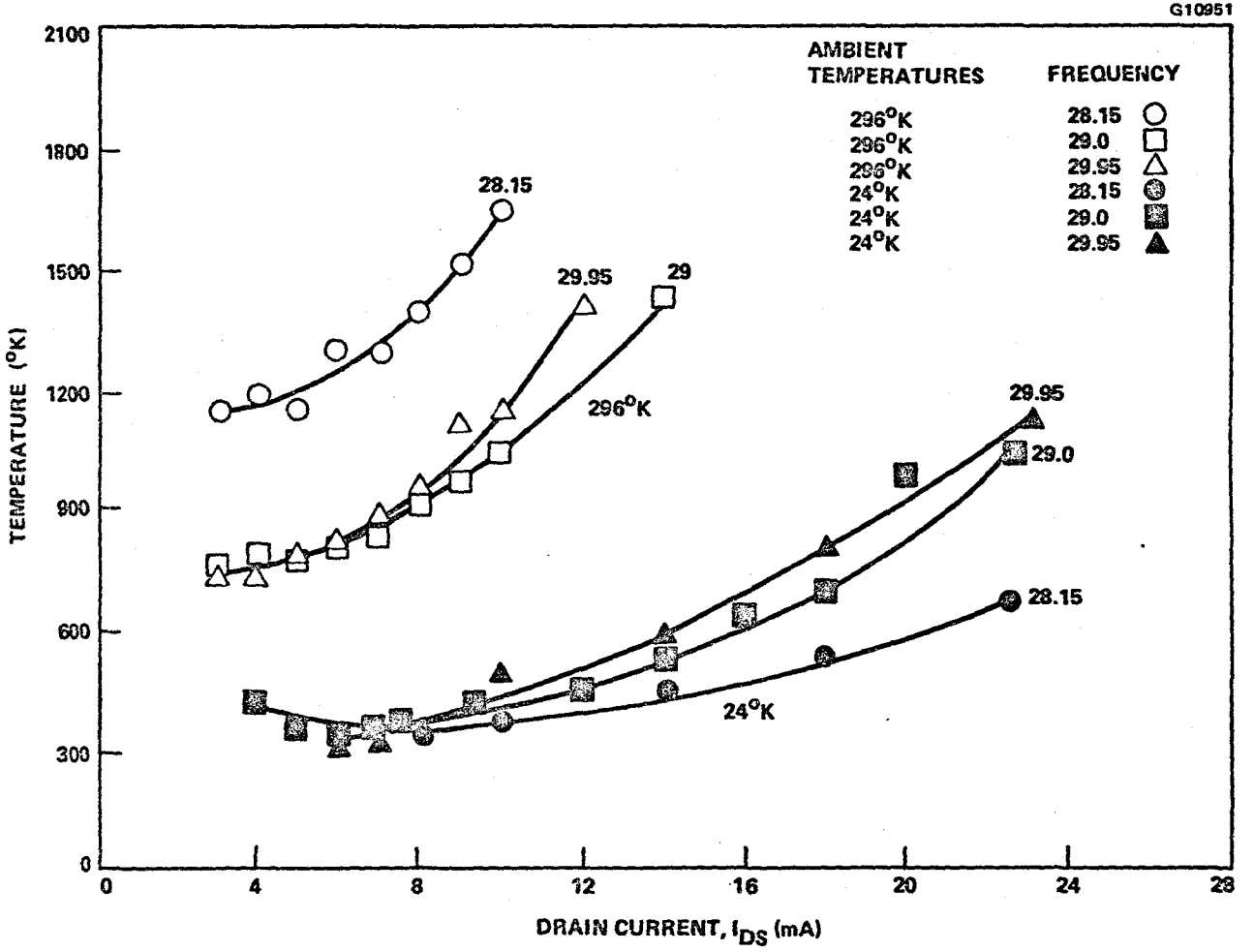

Figure 4-29 Comparison of 296°K and 24°K effective noise temperature.

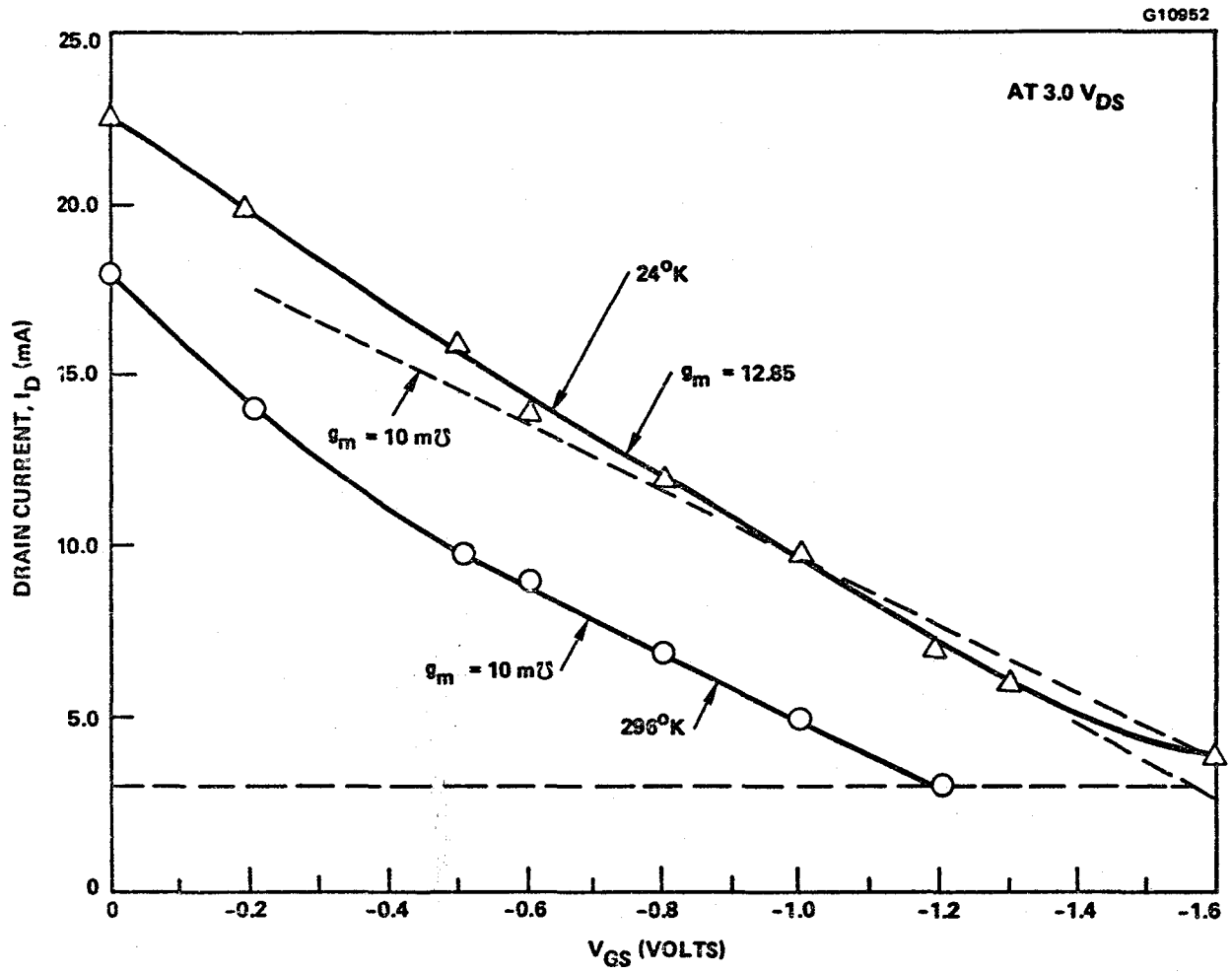

Figure 4-30 Drain current versus gate voltage at 296°K and 24°K.

Similar changes in GaAs device dc characteristics, increased I_{DS} and g_m', have been reported when they were cooled to low temperatures. The increase in I_{DS} could be the result of the increase in saturation velocity, v_s[16], at low temperatures. One unexpected change, an increase in the pinchoff voltage, may have been a surface state effect contributing to an increase in I_{DS}.

A photograph of the amplifier after test completion is shown in Figure 4-31. The microstrip circuit consists of Cr-Au metallization on 10 mil thick, fused quartz substrates. The network was tuned by parallel gap-welding gold foil and the circuit. Parallel plate chip capacitors and 0.7 mil bond wire also were used to construct the RF matching and dc bias networks. The center mount, waveguide-to-microstrip transition mount and walls were fabricated from brass. The amplifier carrier was Invar. The transitions were connected to the amplifier with gold ribbon gap welded between the microstrip lines.

After test completion the unit was carefully examined to determine failure points in the assembly. All circuitry mounted on the Invar carrier, including the gap welds on the matching network and transitions, remained intact. Failure points occurred on the transitions as evidenced by the fracturing of the fused quartz substrates in both transitions. We believe that this is the result of joint stress at the waveguide-to-waveguide mount interface. Additionally, though it cannot be seen in the photograph, one of the transition substrates is partially lifted, indicating an epoxied bond failure.

Attempts to measure several type 1 amplifiers were unsuccessful due to stability problems which resulted in high frequency oscillations. Attempts to suppress the oscillations failed, but indicated an excess of 40 GHz in the fundamental oscillation frequency.

Generally, the agreement between the room temperature measurements at TRC and NRL was worse than expected. This may have been due to differences in source and load impedances presented by the different test systems, differences in the actual DSB measurement or mechanical damage to the units during transportation.

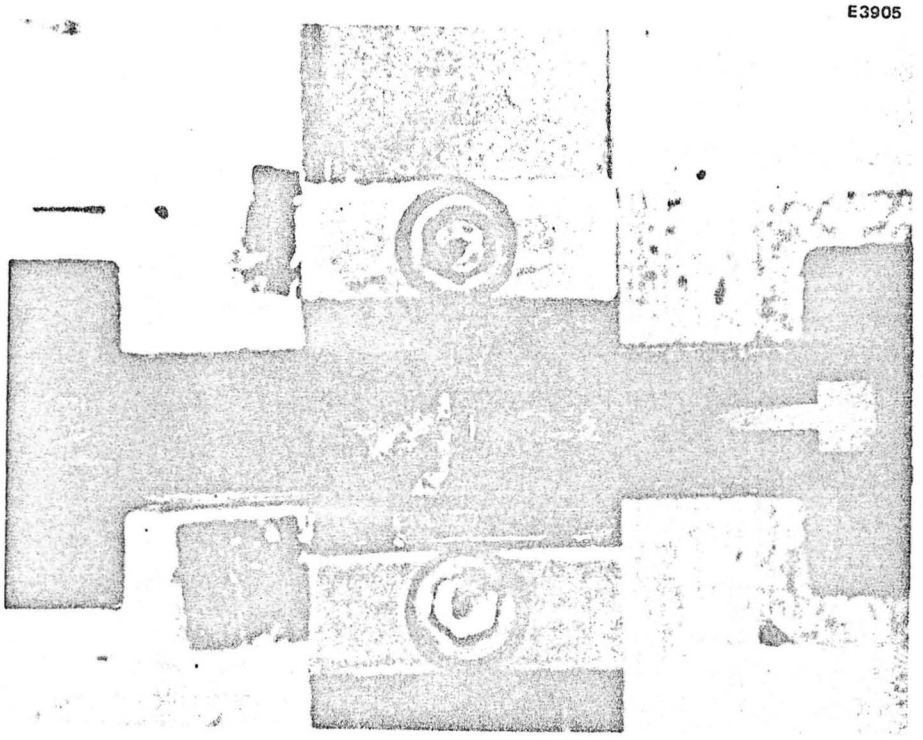

Figure 4-31 30 GHz amplifier after cryogenic tests.

4.2 IMAGE REJECTION FILTER

The frequencies of interest in the mixing process are summarized below.

Local Oscillator (LO)	25 GHz
LO Harmonics	N(25.0) GHz
Signal (L.O. + I.F.)	27.5 to 30.0 GHz
Image (L.O. - I.F.)	20.0 to 22.5 GHz
Intermediate (I.F.)	2.5 to 5.0 GHz

A filter is required to eliminate noise and spurious signals from entering the mixer and being down converted to the IF band. In this section, the design and the development of the image rejection filter is presented.

4.2.1 Filter Design and Implementation

The image rejection filter was implemented in the form of a parallel-coupled microstrip bandpass filter. This filter configuration was chosen for its simplicity, suitability for microstrip implementation, ease of fine tuning, and ability to achieve the necessary bandwidth with realizable elements. The design goals of the filter are listed below:

Passband	27.5 to 30.0 GHz	Minimum insertion loss
Image	20.0 to 22.5 GHz	20 dB rejection
LO	25.0 GHz	Maximum rejection

To achieve low insertion loss, a minimum number of resonators (2) were selected. The design values for a Tchebyscheff response with 12 percent bandwidth and 0.2 dB ripple were obtained using the equations given by Matthaei[17] for filters with $\lambda/4$ wavelength resonators. Corrections for end effects and line width changes were applied during the filter layout. The equivalent circuit of the filter is shown in Figure 4-32 and its computed performance is illustrated in Figure 4-33.

A photograph of the filter is shown in Figure 4-34. The circuits were fabricated on a 10 mil thick fused quartz substrate with Cr-Au metallization. The pattern was etched using an ion milling technique to maintain edge acuity and gap spacing.

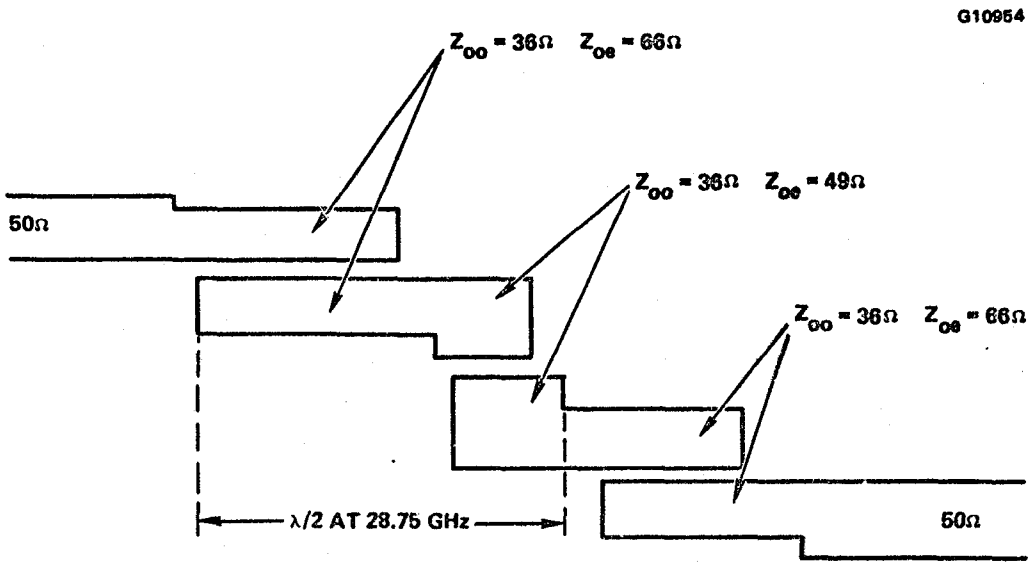

Figure 4-32 Equivalent circuit for microstrip bandpass filter.

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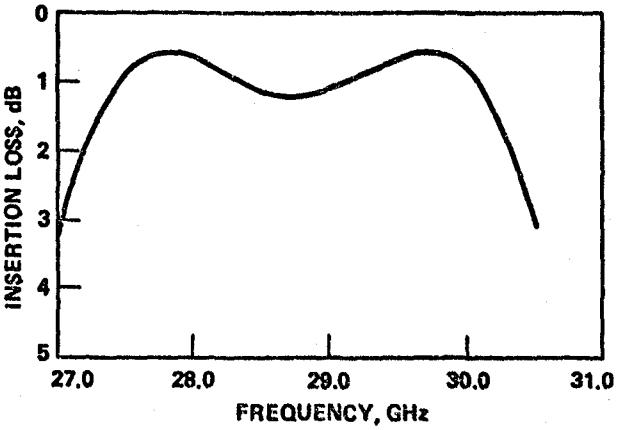
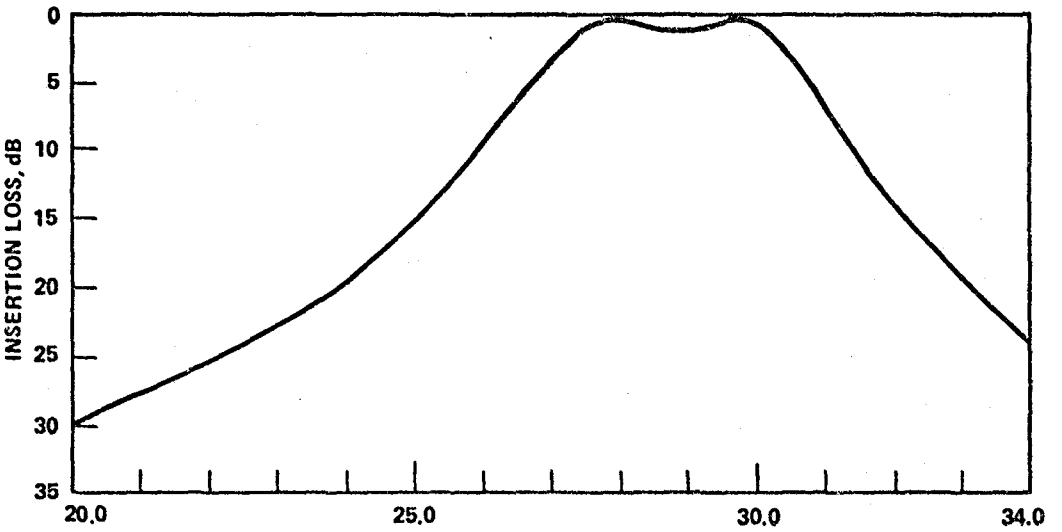


(a) PASS BAND INSERTION LOSS



(b) FREQUENCY PERFORMANCE OF IMAGE REJECTION FILTER

Figure 4-33 Computed image rejection filter performance.

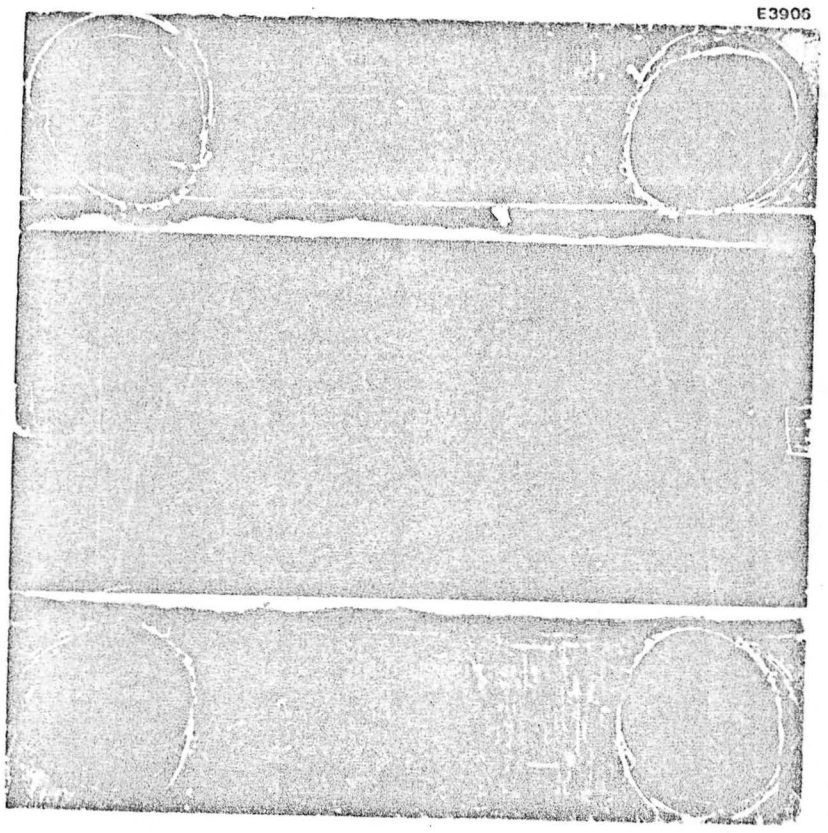


Figure 4-34 Microstrip bandpass filter.

4.2.2 Filter Performance

The performance of the filter is shown in Figure 4-35. The insertion loss is 1.2 dB in the passband which is centered at 27.8 GHz, 3 percent off the design goal. The 1-dB bandwidth is 2.5 GHz. The return loss over the band is greater than 20 dB. The filters were tuned to the 28.75 GHz center frequency by reducing the length of the resonators. This was performed using a laser trimming system. The frequency response of a tuned filter is shown in Figure 4-36. The insertion loss, 1.0 dB $\pm$ 0.3 dB over the band, is in excellent agreement with the design simulation. The 1-dB bandwidth of the completed unit is 16 percent lower than the simulation but covers the required frequency range. A Q of 150 for the microstrip resonators can be calculated from the measured insertion loss and bandwidth and compares favorably with theoretical estimates.

The frequency response of a tuned filter over a broader bandwidth is shown in Figure 4-37. The passband insertion loss is 1 dB with a 12 percent 3 dB bandwidth. Rejection at the 25 GHz LO frequency is 15 dB and at image frequencies (20.0 to 22.5 GHz) is 23 to 29 dB.

4.3 DUAL-GATE FET MIXER

Dual-gate FETs provide an alternative to diodes and single gate FETs for mixer applications, in particular, where low LO drive and conversion gain are desired. By introducing a different signal on each gate, a simple effective means for modulating the device current at two frequencies is obtained that eliminates coupler requirements and simplifies matching network design. This section will outline general dual-gate mixer design criterion, describe its implementation and summarize the results achieved on units developed during this program.

4.3.1 Design Consideration

The dual-gate mixer performance goal includes an RF frequency range from 27.5 to 30.0 GHz with the RF to IF conversion gain of 11 dB. The SSB noise figure goal was 12 dB. Initially, the LO and IF frequencies were unspecified and later

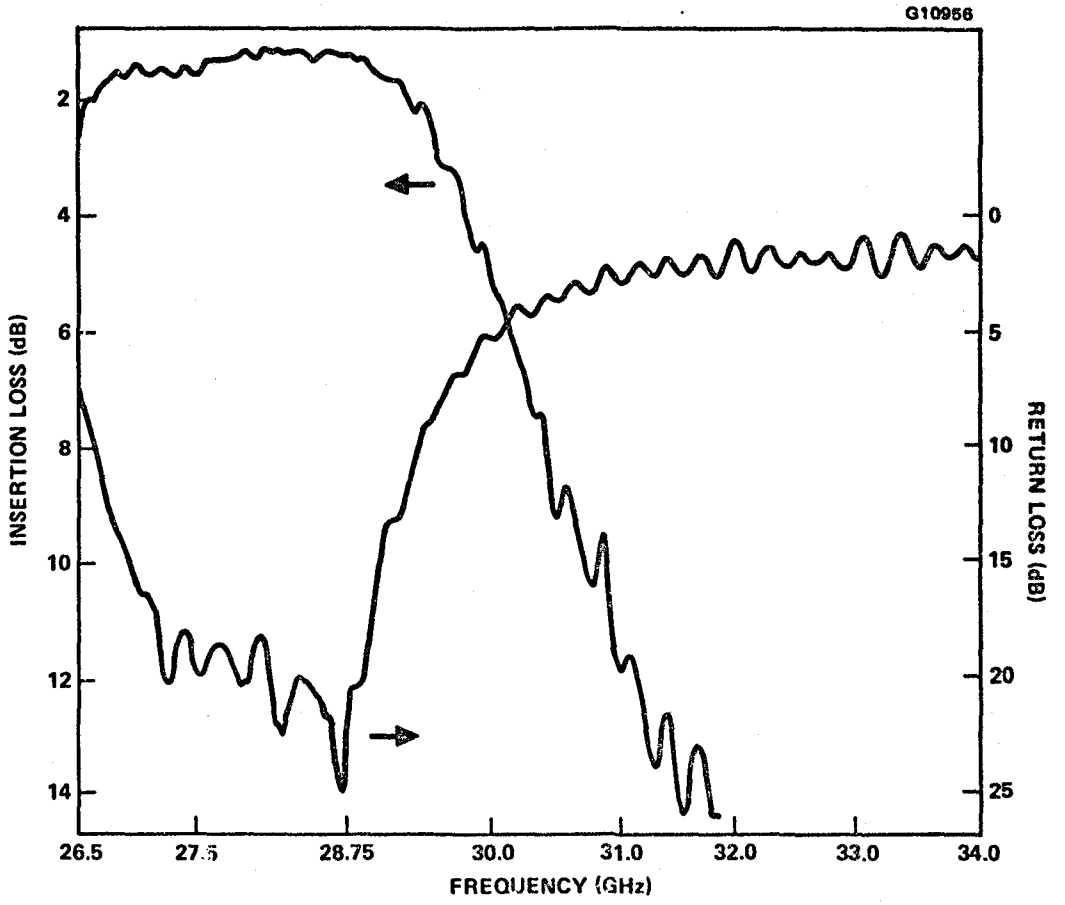


Figure 4-35 Frequency response of microstrip bandpass filter.

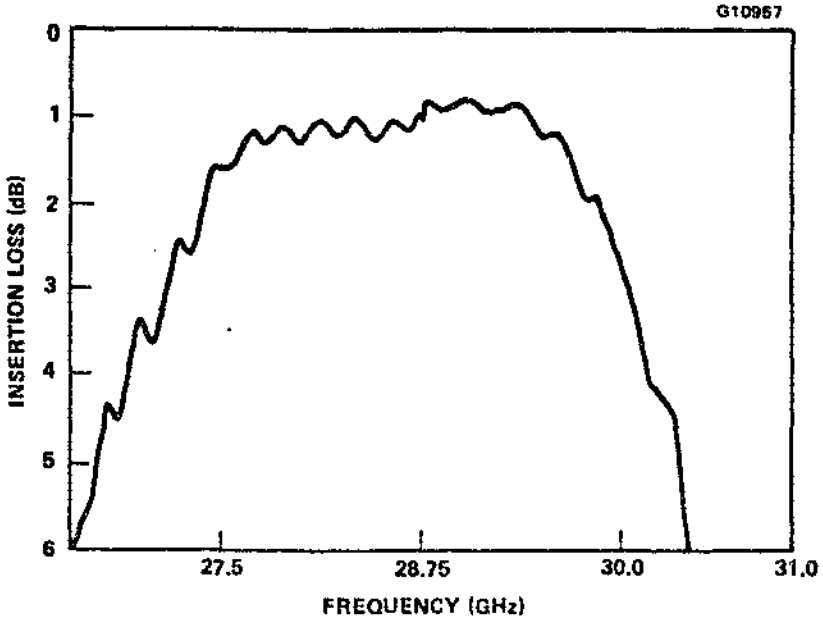


Figure 4-36 Passband response of a tuned filter.

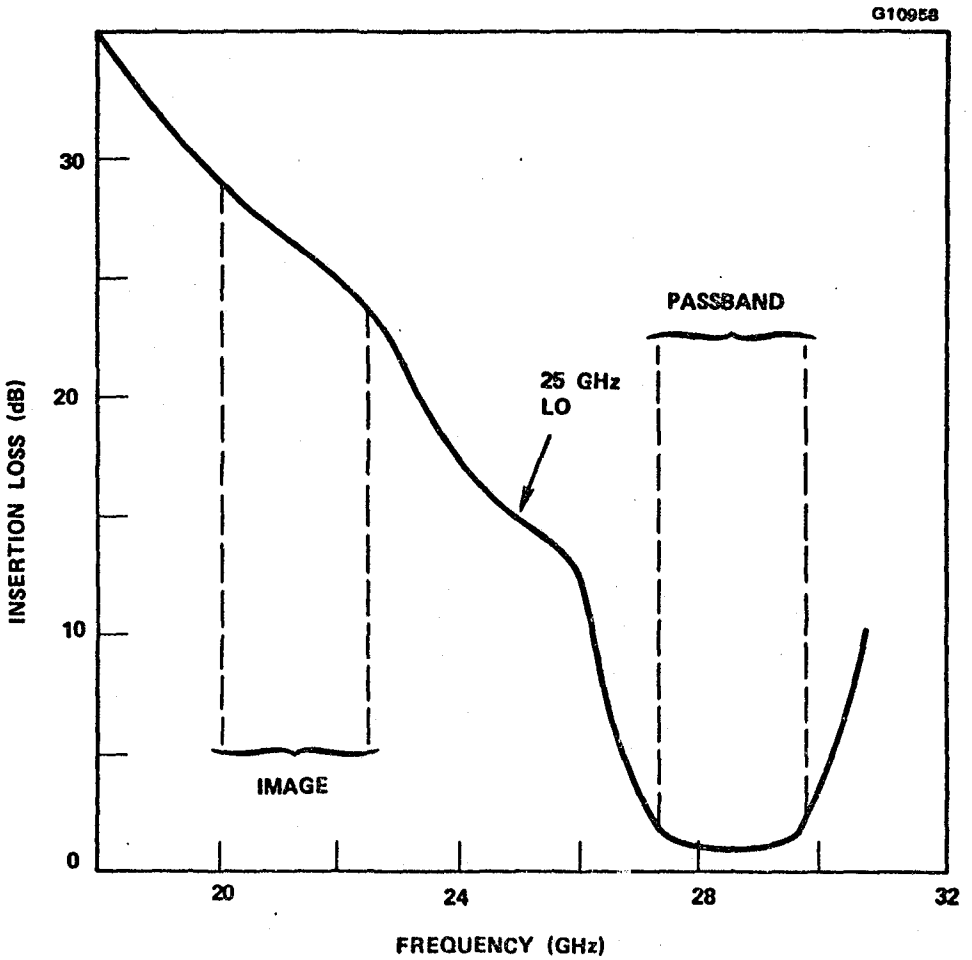


Figure 4-37 Bandpass filter frequency response.

chosen to be 25.0 GHz and 2.5 to 5.0 GHz, respectively. Due to the octave bandwidth requirement, difficulty with the dual-gate FET IF port matching was anticipated. The problem of determining the optimum noise terminations at the dual-gate mixer ports and their interaction was also unknown at these frequencies.

The mixing action in a single-gate FET is primarily a result of the modulation of the device transconductance, g_m.[18] The conversion gain is the highest for the device biased near pinchoff, since g_m variation is strongest there. In the dual-gate FET, however, the first gate transconductance, $g_m = g_{m1}$, can be made to vary abruptly with the second gate voltage (Section 3.2). This variation is at least as strong as for a single-gate FET of similar construction.

The analysis of the mixing of two large signals in a nonlinear element is difficult and time consuming. By limiting the magnitude of one of the signals, the problem becomes one of a nonlinear analysis with a single frequency driving function and a linear multifrequency analysis where the nonlinear element has been replaced by a time varying linear impedance.

The mixer design begins with a thorough three-port measurement of the grounded source dual-gate FET under a variety of bias conditions. A LO drive level and bias are selected and g_m is calculated as a function of time. We can express the transconductance as

$$g_m = \sum_{k=-\infty}^{\infty} g_k e^{jk\omega t} \qquad (4.3\text{-}1)$$

where is the local oscillator radian frequency and

$$g_k = \frac{1}{2\pi} \int_0^{2\pi} g_m(t)\, e^{-jk\omega t} dt. \qquad (4.3\text{-}2)$$

We can now replace the nonlinear g_m in the circuit by a time varying linear transconductance. If we introduce a voltage, V_{RF}, across this device, we will get current flow at frequencies $k\omega_{LO} \pm \omega_{RF}$. Classical mixer theory can then be used to analyze the circuit. Pucel [18] has shown that the available conversion gain of a FET is given, approximately, as

$$G_c = \frac{g_1^2 \bar{R}_d}{4\omega_1^2 \bar{C}^2 R_{in}} \qquad (4.3\text{-}3)$$

where g_1 is the conversion transconductance, R_{in} is the input resistance, and C and R_d are the time average values of gate-source capacitance and drain resistance, respectively.

While this was derived for a single-gate FET, it can be applied to the dual-gate device. In the ideal case where g_m of the first gate is a step function when modulated by the second gate, $g_1 = g_m/\pi \approx g_m/3$. Substituting the parameters listed below, which were obtained from DC and small signal measurements on our devices, in equation (4.3-3) a conversion gain of $\sim$5 dB is projected at 28.75 GHz.

$g_m = 20$ m℧ $\qquad R_{in} = 7\,\Omega$

$\bar{R}_d = 900\,\Omega \qquad \bar{C} = 0.12$ pF

A diagram of the dual-gate mixer and a simple equivalent circuit for the device are shown in Figure 4-38. The RF input is impressed on the first gate (closest to the source) and the local oscillator signal is applied to the second gate. The scattering parameter for a device with an inductive gate 2 RF termination was measured as a function of gate 2 DC voltage. The measured data is presented in Table 4-4 and demonstrates the insensitivity of the device input impedance to gate 2 voltage changes, which is typical of this circuit. This advantage allows one to design the input matching network based on small signal data obtained without the LO signal applied.

The IF output is taken from the drain. In addition to providing the low frequency IF matching, the drain circuits must properly terminate the RF signal

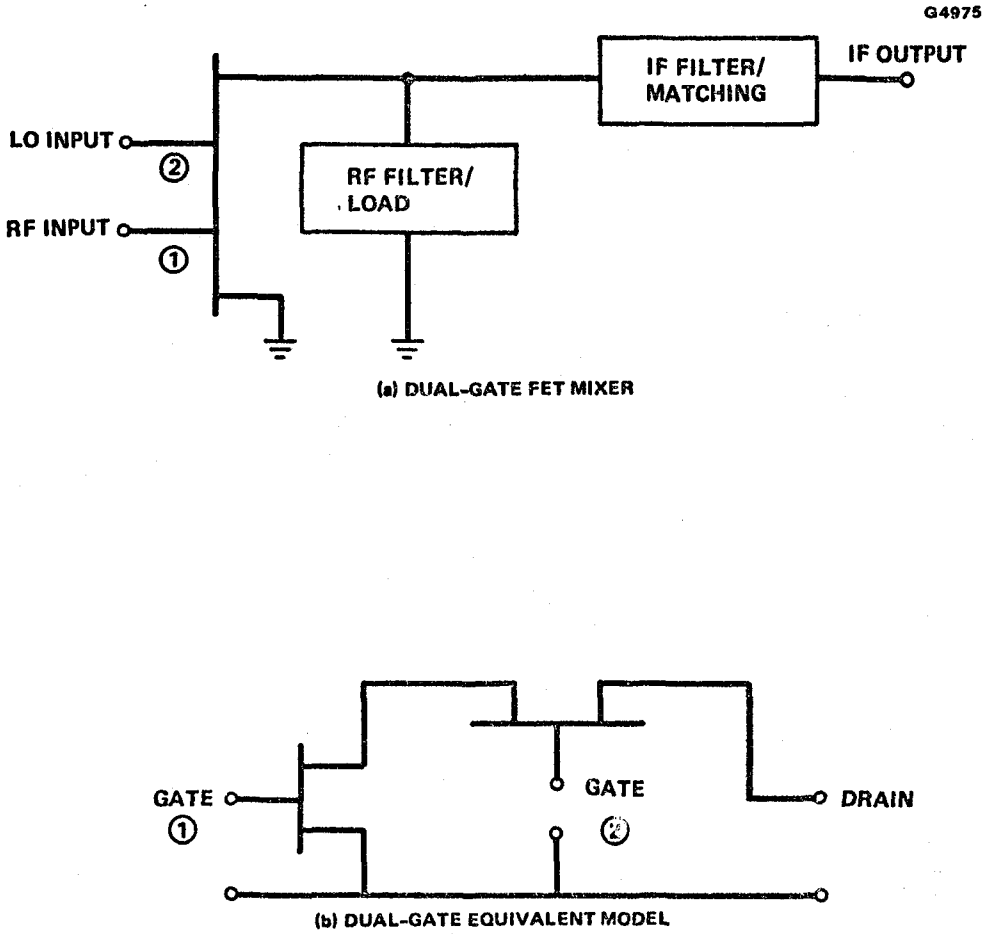


Figure 4-38 Dual-gate mixer schematic and dual-gate FET modeled as two single-gate FETs in cascade.

TABLE 4-4

S-PARAMETERS OF DUAL-GATE FET AS A FUNCTION OF GATE 2 BIAS POINT

Input Parameters

Bias		Frequency		
V_{G2} Volts	I_D mA	2.0 GHz Mag-Angle	10.0 GHz Mag-Angle	18.0 GHz Mag-Angle
+0.9	36	1.00 < -8.6°	0.94 < -63°	0.83 < -82°
0.0	27	1.00 < -8.8°	0.95 < -65°	0.85 < -89°
-0.5	21	1.00 < -8.7°	0.95 < -65°	0.86 < -90°
-1.0	13	1.00 < -8.4°	0.94 < -63°	0.83 < -82°
-2.0	5	1.00 < -10.2°	0.96 < -63°	0.87 < -97°

Output Parameters

Bias		Frequency		
V_{G2} Volts	I_D mA	2.0 GHz Mag-Angle	10.0 GHz Mag-Angle	18.0 GHz Mag-Angle
+0.9	36	0.93 < -2.8°	0.92 < -27°	0.95 < -48°
0.0	27	0.89 < -2.8°	0.89 < -28°	0.93 < -52°
-0.5	21	0.86 < -2.8°	0.86 < -28°	0.92 < -53°
-1.0	13	0.93 < -2.8°	0.92 < -27°	0.95 < -48°
-2.0	5	0.85 < -3.0°	0.84 < -29°	0.87 < -56°

frequencies and LO frequency to prevent instability, optimize the mixer noise figure, gain, maintain linearity and minimize the LO drive power. Unlike the input, the output impedance of the device varies considerably with gate 2 voltage, indicating that the drain match will be sensitive to the LO drive level. Device output S-parameter measurements as a function of V_{G2} are tabulated in Table 4-4.

4.3.2 Mixer Circuit Description

A photograph of the dual-gate mixer circuit is shown in Figure 4-39. The dimensions of the mixer are 0.060x0.250x0.700 inches. The matching circuits are fabricated on one quartz substrate, 10 mils thick, with Cr-Au metallization. A hole was ground through the substrate for mounting the device. The device and circuit are epoxied to the nickel and gold plated invar carrier. High dielectric constant chip capacitors are used for dc blocking and RF bypassing on the circuit. Bond wires 0.7 mil in diameter are used for inductive elements and $\lambda/4$ transmission lines. The RF and LO signals were introduced to the device from opposite sides of the carrier, a configuration simplifying the interconnection of the circuit to the device bonding pads. The carrier incorporates a microstrip-to-coaxial transition through the bottom of the carrier for the IF. An approximate equivalent circuit of the mixer is shown in Figure 4-40.

A photograph of the dual-gate mixer mounted in the test fixture is shown in Figure 4-41. The carrier is mounted between two waveguide-to-microstrip transitions, one K-band and one Ka-band. The test fixture provides dc bias and an SMA coaxial IF output port.

4.3.3 Mixer Performance

Initially the RF conversion loss of the mixer was quite high, typically 10 dB. These early mixers did, however, exhibit the low level LO drive requirements (1.1 dBm) as expected. The RF port matching was generally not very difficult with a typical return loss of greater than 12 dB over the band.

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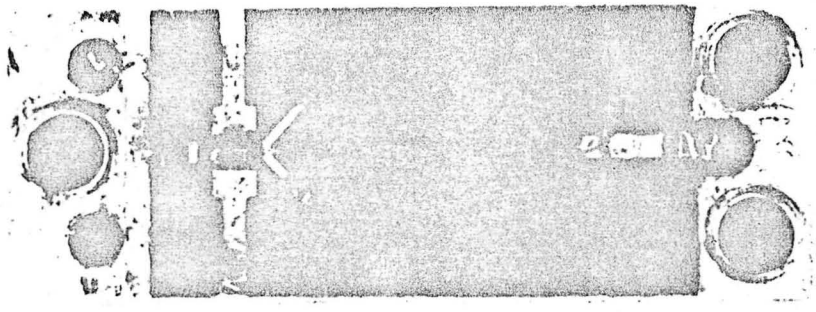

Figure 4-39 30 GHz dual-gate FET mixer carrier.

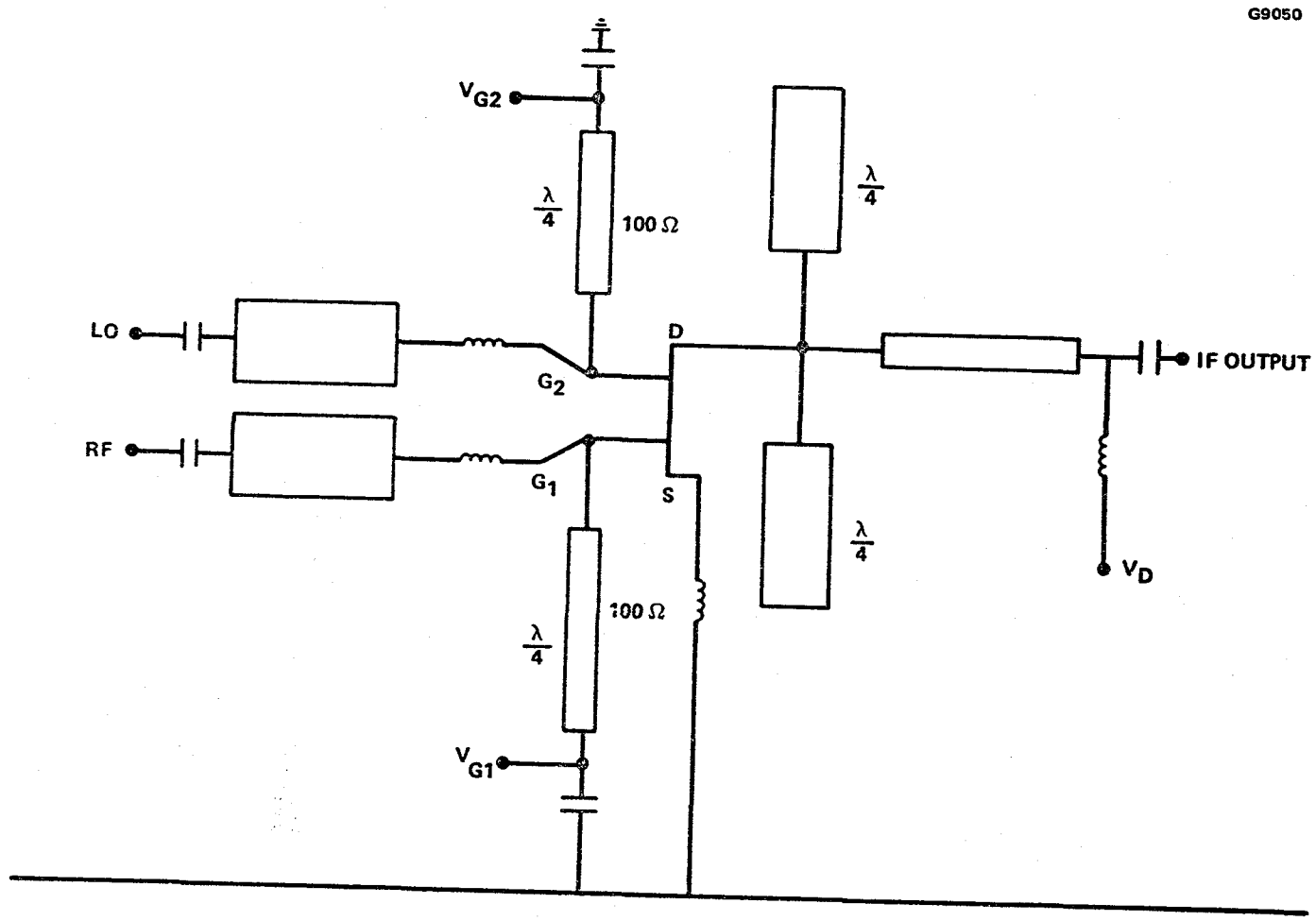

Figure 4-40 Ka-band mixer topology.

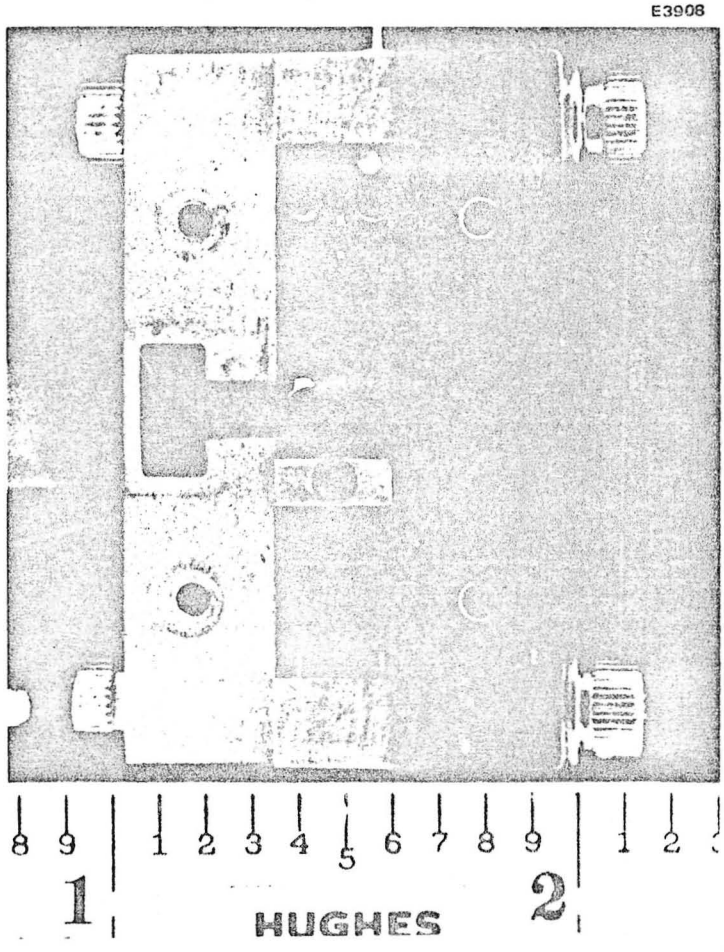

Figure 4-41 An assembled Ka-band dual-gate FET mixer.

The frequency performance of a dual-gate mixer developed later in the program is shown in Figure 4-42. Due to improved devices and circuit techniques, the noise figure is reduced to 10 dB at band center. The maximum conversion gain is +0.5 dB and is achieved at band center. The narrow conversion bandwidth was typical of all the optimized mixers. This is a result of the IF port matching network. The IF port of the device presents a very high impedance and is difficult to match over any wide bandwidth without a complex multi-element network. Due to space limitations, this was not possible. The mixer noise figure is determined primarily by the RF port matching. The performance of the mixers at 29 GHz is summarized in Table 4-5; twelve mixers were evaluated. Typically, the signal level of the external 25 GHz LO was +9 dBm. The average conversion loss was approximately 3 dB but the units produced later in the program tended to be better. The highest conversion gain achieved was +3 dB. The best noise figure measured was 10 dB with +0.5 dB conversion gain. Generally, the port-to-port isolation was greater than 20 dB for any of the ports.

A few problems were encountered during the mixer development process which need further investigation. One problem, with a significant impact on the operation and optimization of the mixers, was the variation in optimum bias condition for best conversion. The twelve mixers constructed and evaluated, generally, exhibited two bias conditions which resulted in near equal performance; one at high and one at low operating currents. The final optimized operating current of the mixers varied from 1 mA to 30 mA with most at low current bias points. The optimum bias conditions for the mixers are shown in Figure 4-43. The best result, +3.0 dB, was obtained with a V_{G2} = +1.0 V. However, for V_{G2} > +1.0 V, the device was unstable for some bias conditions and for some matching conditions demonstrated non-linear mixing characteristics.

Another problem which made the mixer measurements and circuit tweeking very difficult was the interaction between the gates. This made optimizing the RF and LO gate matching independently very difficult.

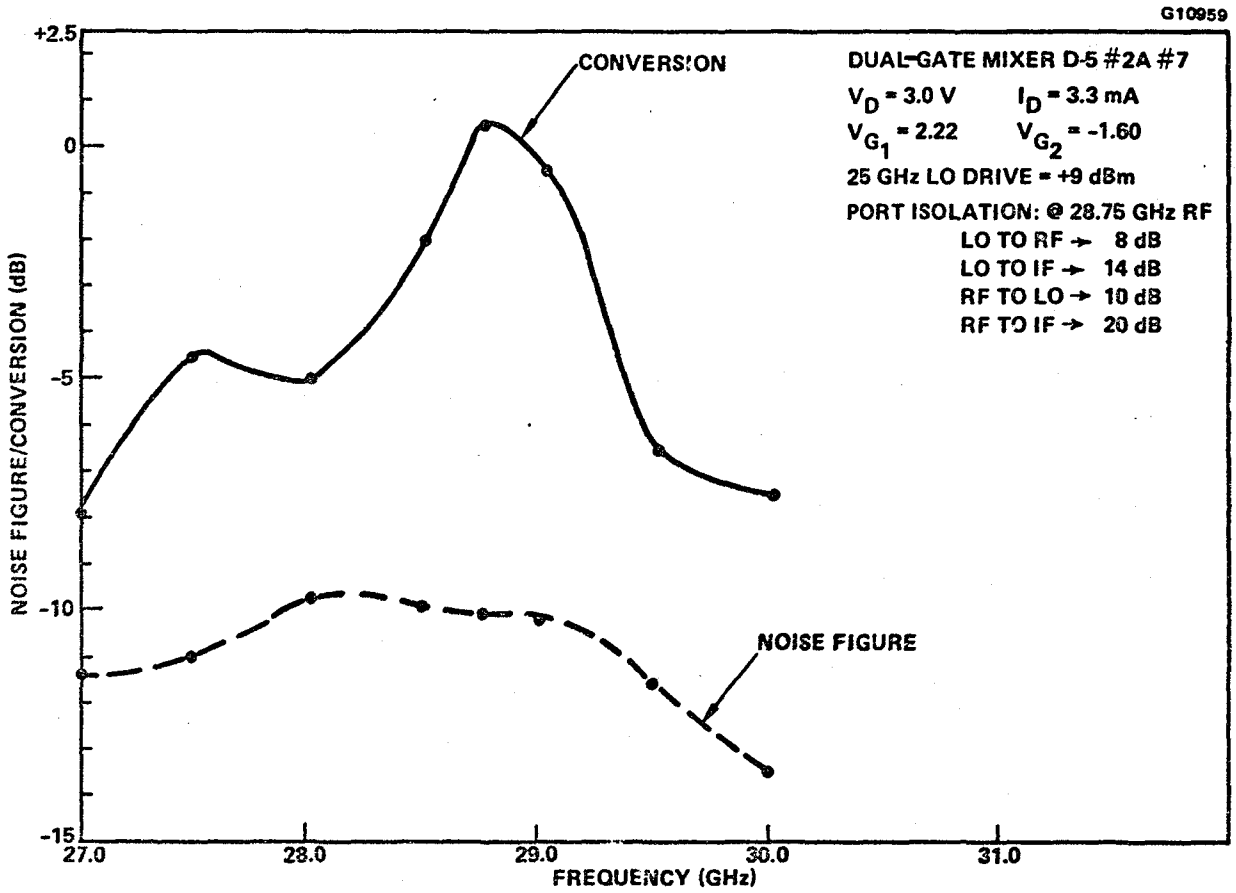

Figure 4-42 Frequency response of Ka-band dual-gate FET mixer.

TABLE 4-5

PERFORMANCE SUMMARY OF DUAL-GATE FET MIXERS AT 29 GHz

Mixer #	Conversion Gain (dB)*	Noise Figure, (dB)*	RF to IF (dB)	Isolation LO to IF (dB)	LO to RF (dB)
D-2	-10 **	--	--	--	--
D5A #3	+3.0	--	--	--	--
D52A #7	+0.5	10.0	-20	-14	-8
D5 #1A	-5.5	11.7	-33	-28	-30
D5 #2A	-6.5	16.0	-26	-23	--
D5A9	-6.0	--	--	--	--
D5-A	-4.0	--	--	--	--
D52A #2	-2.5	15.0	--	--	--
D5	-7.0	--	--	--	-5
D6A8	-2.0	15.0	--	--	--
D6 #1A	-4.4	16	-43	-25	-20
D6 #1	-0.4	--	-51	-32	-19.5

*@ +9 dBm LO drive level
**@ +1.1 dBm LO drive level

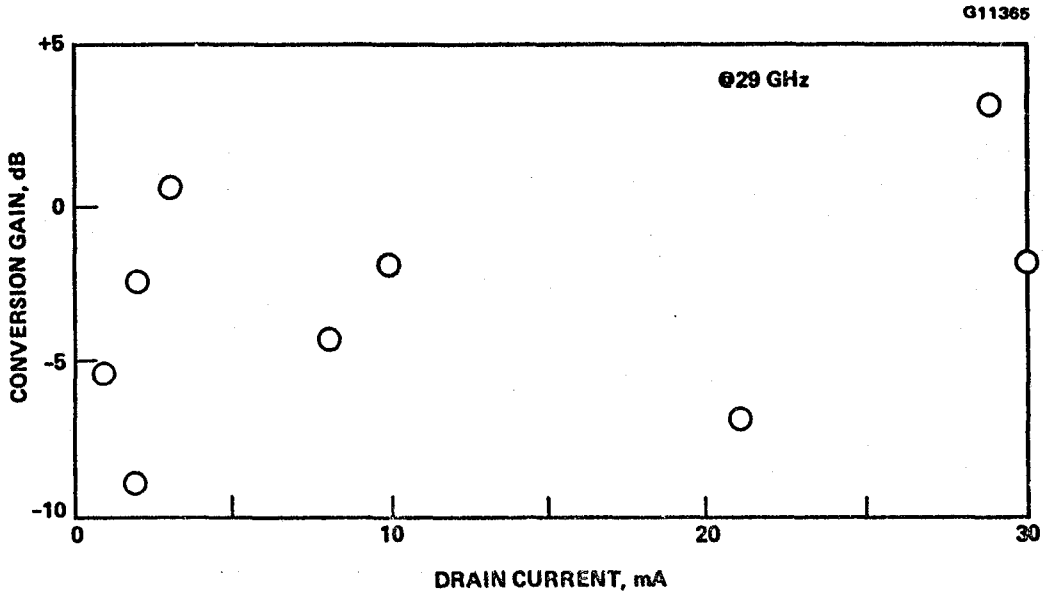

Figure 4-43 Optimum conversion versus operating current for several dual-gate FET mixers.

4.3.4 Summary

During this program, significant progress was made on the dual-gate FET mixer. The mixer noise figure specification was realized and the conversion gain, though below the design goal, was improved as experience and device improvements progressed. It is clear that a more complicated (multiple pole) IF matching network and a higher IF frequency will be required to achieve the 2.5 GHz IF bandwidth requirement.

4.4 LOCAL OSCILLATOR DEVELOPMENT

In this section, the design approach for a low phase noise 25 GHz FET local oscillator is presented. The basic oscillator configuration is presented first followed by phase noise considerations and the oscillator circuit configuration. The design goals are listed in Table 4-6.

4.4.1 FET Colpitts Oscillators

Microwave oscillators can generally be reduced to the basic Colpitts configuration shown in Figure 4-44. Here, the frequency of oscillation is set by the resonant frequency of the LC loop with the FET acting as the active source sustaining the loop current. The capacitances, C_1 and C_2 in the figure, are internal device interelectrode capacitances which are simply incorporated into the oscillator circuit. Any of the three device terminals can be connected to

TABLE 4-6

FET OSCILLATOR PERFORMANCE GOALS

Frequency	25 GHz
LO Power	+10 dBm
Phase Noise	2° rms integrated from 10 kHz to 100 kHz from the carrier
Freq/Temp. Coefficient	1 MHz/$^{\circ}$C

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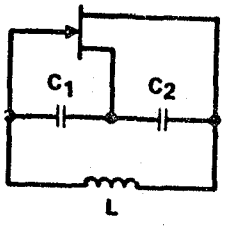
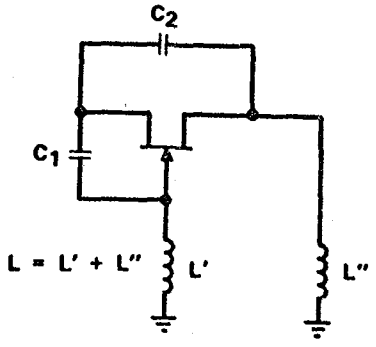


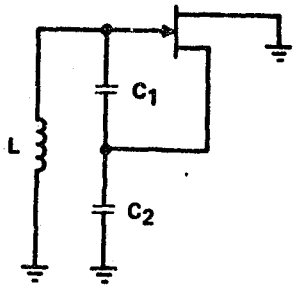
$$\omega_o = \frac{1}{\sqrt{LC}}$$

$$\frac{1}{C} = \frac{1}{C_1} + \frac{1}{C_2}$$

a) BASIC COLPITTS OSCILLATOR



b) COMMON GATE



c) COMMON DRAIN

Figure 4-44 FET oscillator circuits.

ground; the circuit is still analyzed as a Colpitts oscillator. The selection of which terminal to connect to ground should be made based on the ease of coupling to the load, effects of parasitics and thermal considerations.

Two popular oscillator configurations, the common gate and the common drain, are also shown in Figure 4-44. In both, configuration C_1 is usually the internal gate-to-source interelectrode capacitance. C_2 is also often internal. In the common gate and common drain configurations, the load is usually coupled to the oscillator at the drain and source terminals, respectively. To oscillate, the Colpitts oscillator simply requires a net inductive reactance connected between the gate and drain. As described below, we prefer the common gate configuration since it minimizes parasitics and allows the load to be easily coupled into the circuit. This basic configuration has been employed at Hughes with FET oscillators operating at fundamental frequencies up to 36 GHz.

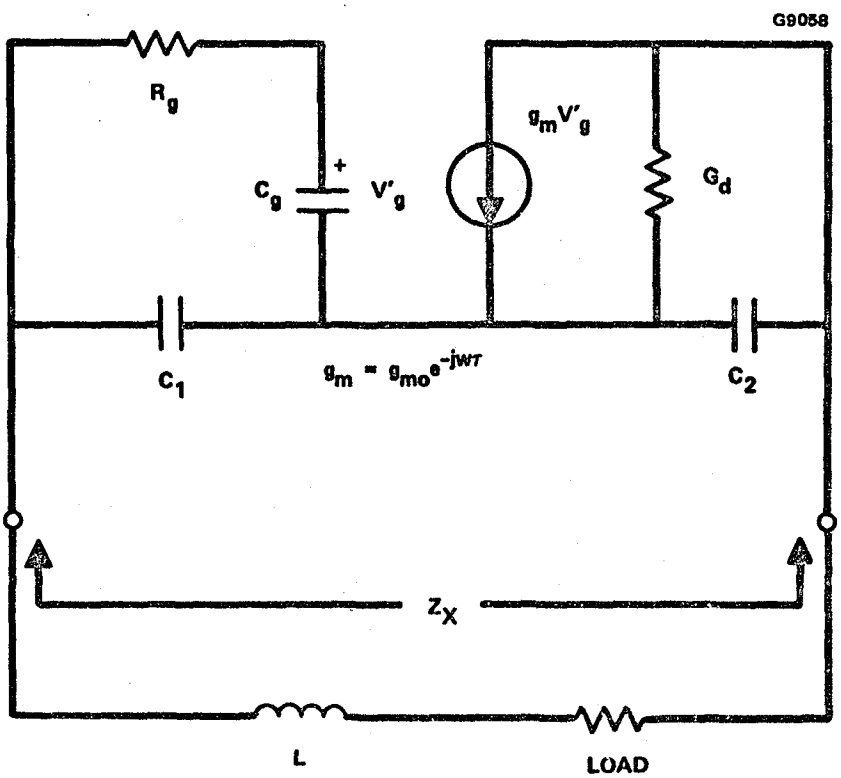
The Colpitts oscillator circuit was analyzed to determine its frequency limits and the impact of device parameters on that limit. The oscillator configuration and FET parameters are defined in Figure 4-45. The fundamental condition for oscillations is that the real part of Z_x in the figure must be less than zero. When the real part of Z_x ceases to be negative, oscillations can no longer exist. Solving for the frequency which results in

$$R_e [Z_x] = 0 \qquad (4.4\text{-}1)$$

yields the maximum frequency of oscillation. This procedure is summarized in Figure 4-46. The most significant result of this analysis is that f_{max} is limited by the gate propagation delay τ as

$$\omega_{max} < \frac{\pi}{2} \frac{1}{\tau} \qquad (4.4\text{-}2)$$

Other parasitic impedances further reduce the practical f_{max} far below this limit. For example, with a 0.5 μm gate length FET (τ = 3 ps), f_{max} is limited to 83 GHz by propagation delay. However, due to parasitic effects, f_{max} is practically limited to approximately 60 GHz.



FUNDAMENTAL OSCILLATION CONDITION:

$$R_e[Z_X] < 0$$

Figure 4-45 FET oscillator equivalent circuit.

G11366

ω_{max} DETERMINED FROM:

$$R_e [Z_X] = 0$$

TRANSCENDENTAL EQUATION FOR ω_{max}:

$$(-\omega_T C_2 \cos\Phi_\tau + G_d)\,\omega_{max} + (C_1 + C_2)\,C_2 R_g \omega^3_{max} - \omega_T G_d \sin \Phi_\tau \sim 0$$

WHERE $\Phi_\tau = \omega_{max}\,\tau$

$$\omega_T = \frac{g_{mo}}{C_1 + C_g}$$

ω_{max} LIMITED BY:

$$\frac{1}{\tau} \cos^{-1} \frac{G_d}{\omega_T C_2} < \omega_{max} < \frac{\pi}{2}\,\frac{1}{\tau}$$

τ, THE GATE DELAY, IS A FUNDAMENTAL LIMITATION

Figure 4-46 Maximum frequency of oscillation.

4.4.2 FET Oscillator Phase Noise

The predominate source of oscillator phase noise is upconverted 1/f baseband noise. Hence, the problem of minimizing the oscillator phase noise can be reduced to minimizing the device 1/f baseband noise. Typically, GaAs FETs have very high 1/f noise with a corner frequency of several hundred MHz. There are basically two methods of reducing this flicker noise:

1. GaAs Material Improvements
2. Circuit Techniques

The materials approach has been previously presented in Section 2.0. From a circuit standpoint, minimizing phase noise dictates the following design rules:

1. Maximization of unloaded Q.
2. Maximization of stored reactive energy in the resonator.
3. Signal limiting without degradation of Q.
4. Minimize output power extracted.
5. Choose FET with lowest noise figure at operating frequency and at the actual circuit impedance.
6. Choose a FET with lowest flicker, or 1/f noise.
7. Coupling of output power preferably should be from the resonator.
8. Employ low frequency feedback to stabilize device bias.

Taken together, these requirements indicate that the device should have as large a gate periphery as possible consistent with a low noise figure at the LO frequency. The circuit should use a high Q resonator such as a dielectric resonator. These have been shown to achieve Q's of several thousand at K-band frequencies.

4.4.3 Local Oscillator Design

A photograph of the oscillator circuit is shown in Figure 4-47 and its equivalent circuit is illustrated in Figure 4-48. The oscillator employed a PI-300 VPE device from Lot L191. The oscillator is fabricated on a 25 mil thick alumina substrate. A common gate configuration was selected with the

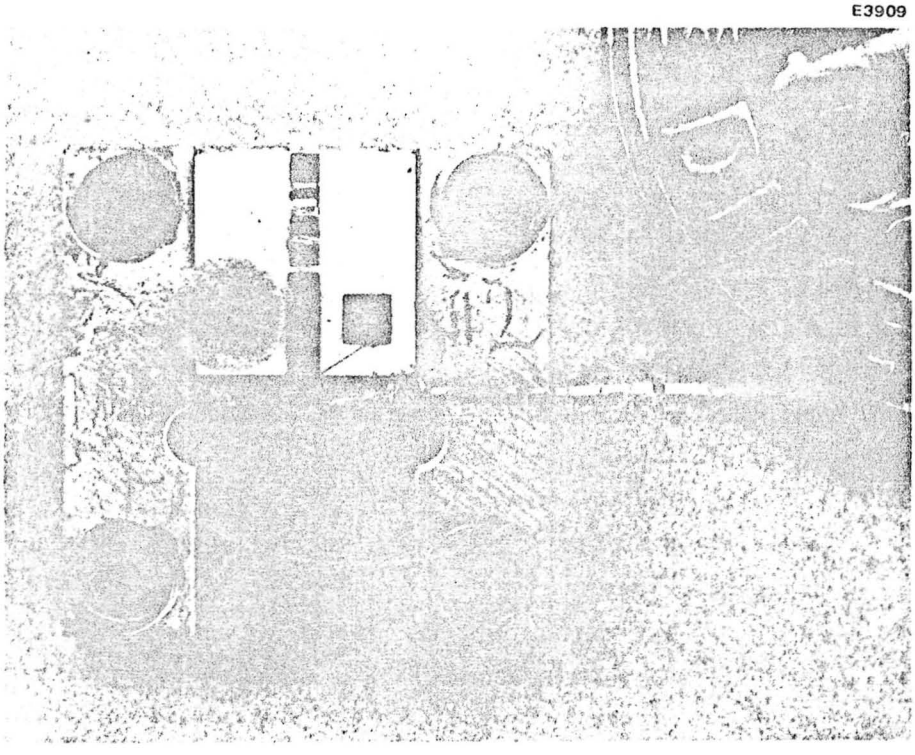


Figure 4-47 25 GHz FET oscillator.

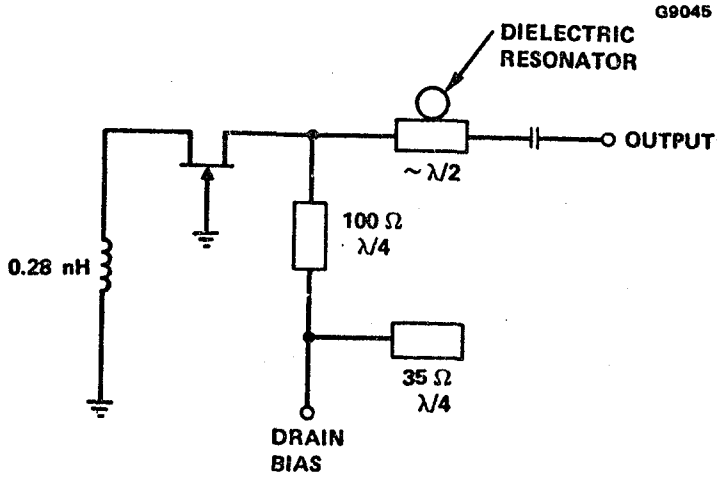


Figure 4-48 Equivalent circuit of FET LO.

resonator and load coupled to the drain. The resonator was coupled by placing it adjacent to the microstrip line approximately a quarter wavelength from an open circuit. The load is capacitively coupled to the oscillator by the gap in the microstrip line. The resonator and load were lightly coupled to the oscillator to maximize Q. For simplicity, the FET device is self-biased at I_{DSS} by a bond wire inductor connected between the source and ground (the gate). This biasing scheme, while simple, prevents us from biasing the gate independently and perhaps further improving the oscillator phase noise.

An important part of the oscillator is the dielectric resonator. It determines the oscillator stability and to a large measure the oscillator phase noise. We obtained a temperature compensated dielectric material, (Zr.Sn) TiO_4, from JFD. The material has a dielectric constant of 38 and an estimated unloaded Q of 2000 at 25 GHz.

The material was obtained in substrate form or pills designed for X-band operation. Since this material is very brittle and cannot be machined easily, a grinding technique was developed to fabricate resonators of the proper dimensions. The dielectric disk resonators were used in the $TE_{01\delta}$ mode; the field configuration as shown in Figure 4-49. To obtain the maximum frequency separation of the various resonator modes, the geometry of the disk must be carefully considered. The optimum L/D ratio is $\approx$0.4 for a maximum frequency separation of the $TE_{01\delta}$ mode from the two next higher modes. Initial resonator designs resulted in unsatisfactory resonators. These initial design equations did not account for the boundary conditions around the resonator. Using the analysis of Dydyk[19] new resonators were constructed with L/D ratios ranging from 0.35 to 0.5 and a measured resonant frequency of 24.4 to 29.7 GHz. The final dimensions of the resonator were determined empirically by hand lapping the resonators until 25 GHz operation was achieved.

4.4.4 Oscillator Performance

The performance of a typical oscillator is summarized in Table 4-7. The oscillator frequency is mechanically tunable ($\pm$100 MHz) by a metal tuning slug which loads the dielectric resonator. The oscillator delivers an output power of typically +10 dBm. The output power of a number of oscillators with a 5.0 V drain

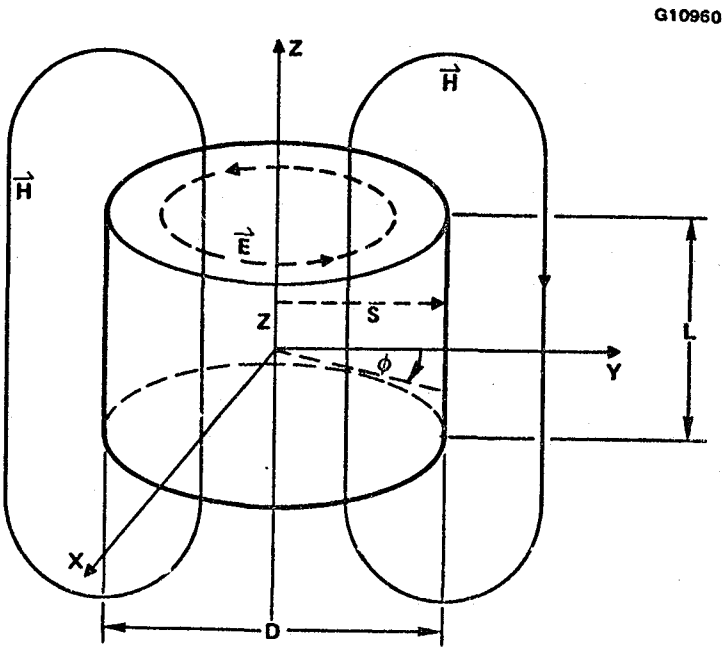


Figure 4-49 Field configuration of dielectric disk at the $TE_{01\delta}$ mode.

TABLE 4-7

PERFORMANCE SUMMARY OF 25 GHz LO

Frequency (Mechanically Tunable)	25 GHz
Output Power	10 dBm
Efficiency	3-5%
Temperature Stability	0.18 MHz/^{o}C
Phase Noise	-50 dBc (100 Hz BW) 25 kHz off carrier
Loaded Q	~350
Frequency Pulling	11 MHz/volt

TABLE 4-8

TABLE OF OSCILLATOR PERFORMANCE @ 25 GHz

Oscillator #	Output Power @ V_D ~5.0 V (dBm)	Device Lot
1	+6.0	---
2	+10.5	MT36
3	+6.0	MT36
4	+9.5	MT36
5	+7.0	L191
6	+7.7	L191
7	+9.5	L191
8	+7.0	L191

bias voltage is listed in Table 4-8. The oscillators are capable of more power, but this would require tighter coupling of the load to the oscillator and a resultant deterioration in the noise performance. They may also be operated at high drain voltages (up to 9 V).

The frequency and power output variation of the oscillator with temperature was measured from -47°C to +26°C. The test configuration is shown in Figure 4-50. While measuring frequency, output power and drain current, the oscillator was slowly lowered into the dewar of liquid N_2 to decrease its operating temperature. The temperature was monitored continuously with a thermocouple mounted to the oscillator housing. Before each measurement was taken, the temperature was allowed to stabilize. With this measurement technique, we achieved a temperature stability of 0.18 MHz/°C (-7 ppm/°C), which is a factor of five better than the required performance of 1 MHz/°C. This was achieved using a resonator with a nominal temperature coefficient of 0 ppm/°C. After obtaining this data, new resonator material was obtained with temperature coefficients of +4 and +10 ppm/°C and incorporated into subsequent oscillators. We believe that the units constructed with this material should demonstrate temperature coefficients of $\pm$3 ppm/°C; however, this was not experimentally confirmed.

While the output power variation was not as consistent and in some cases showed no regular variation, the drain current increased by 10.6 percent when cooled to -47°C. The drain current variation and power variation with temperature is shown in Figure 4-51. The output power increased by approximately 17 percent. An inspection of the units following the tests did not reveal any evidence of degradation or construction failure in the oscillator carrier, device or circuit interfaces and components.

The output spectrum of an oscillator is shown in Figure 4-52. The single sideband phase noise is approximately -50 dBc in a 100 Hz bandwidth 25 kHz from the carrier.

The RMS phase noise in a given bandwidth can be expressed in terms of the power spectrum $\mathcal{L}(f_m)$ as

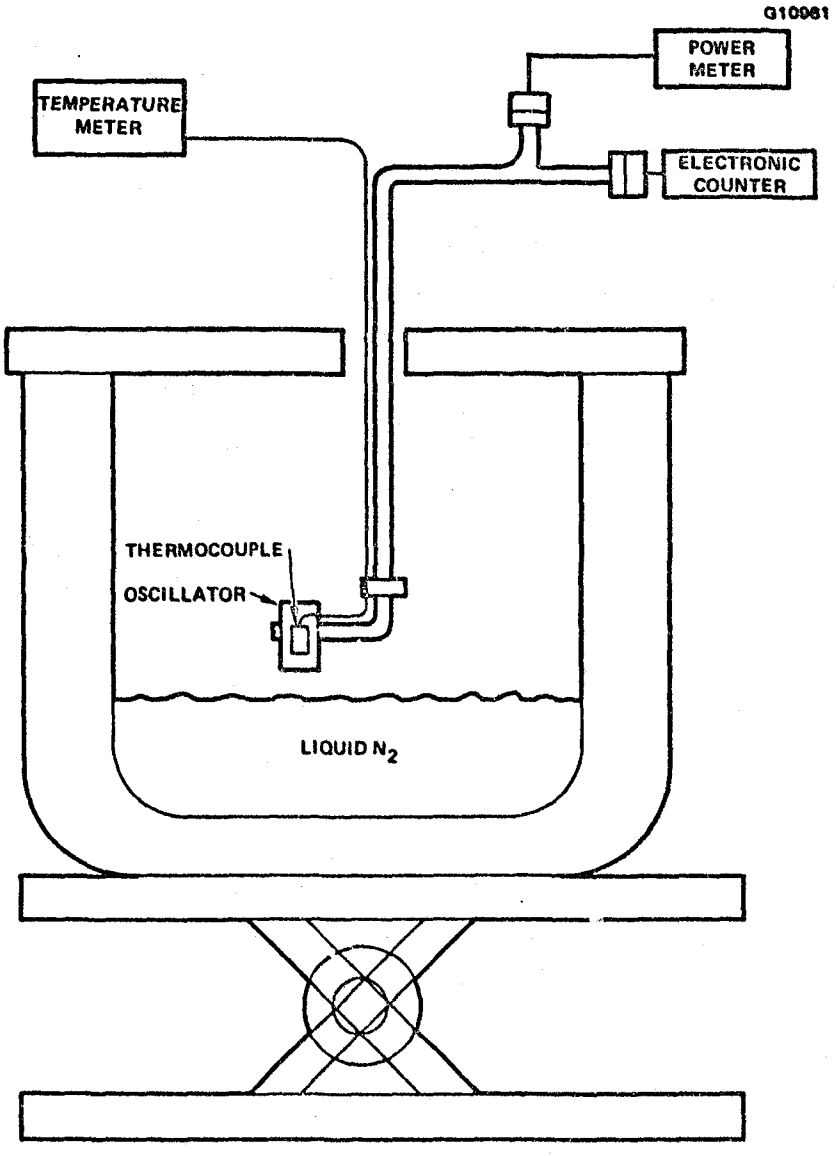


Figure 4-50 Schematic of oscillator temperature test.

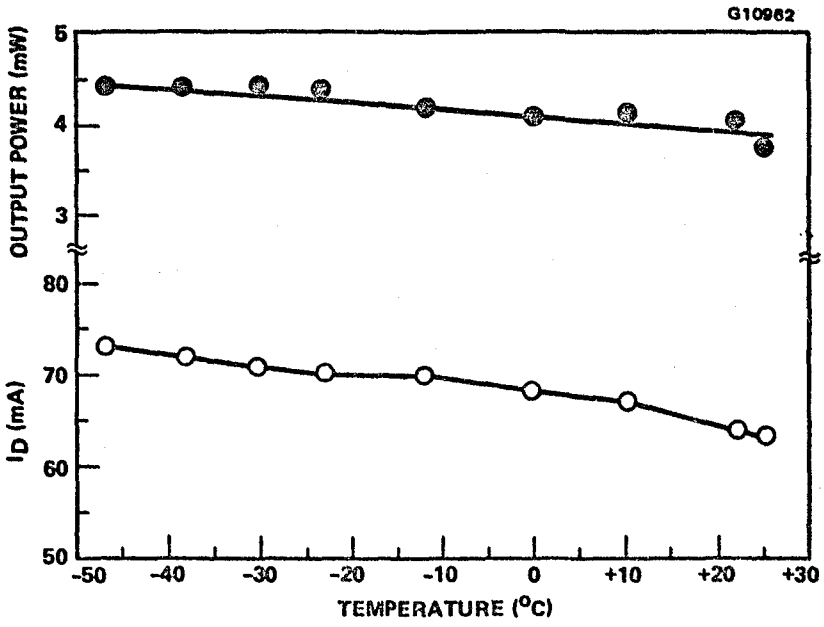


Figure 4-51 Drain current and output power variation with temperature.

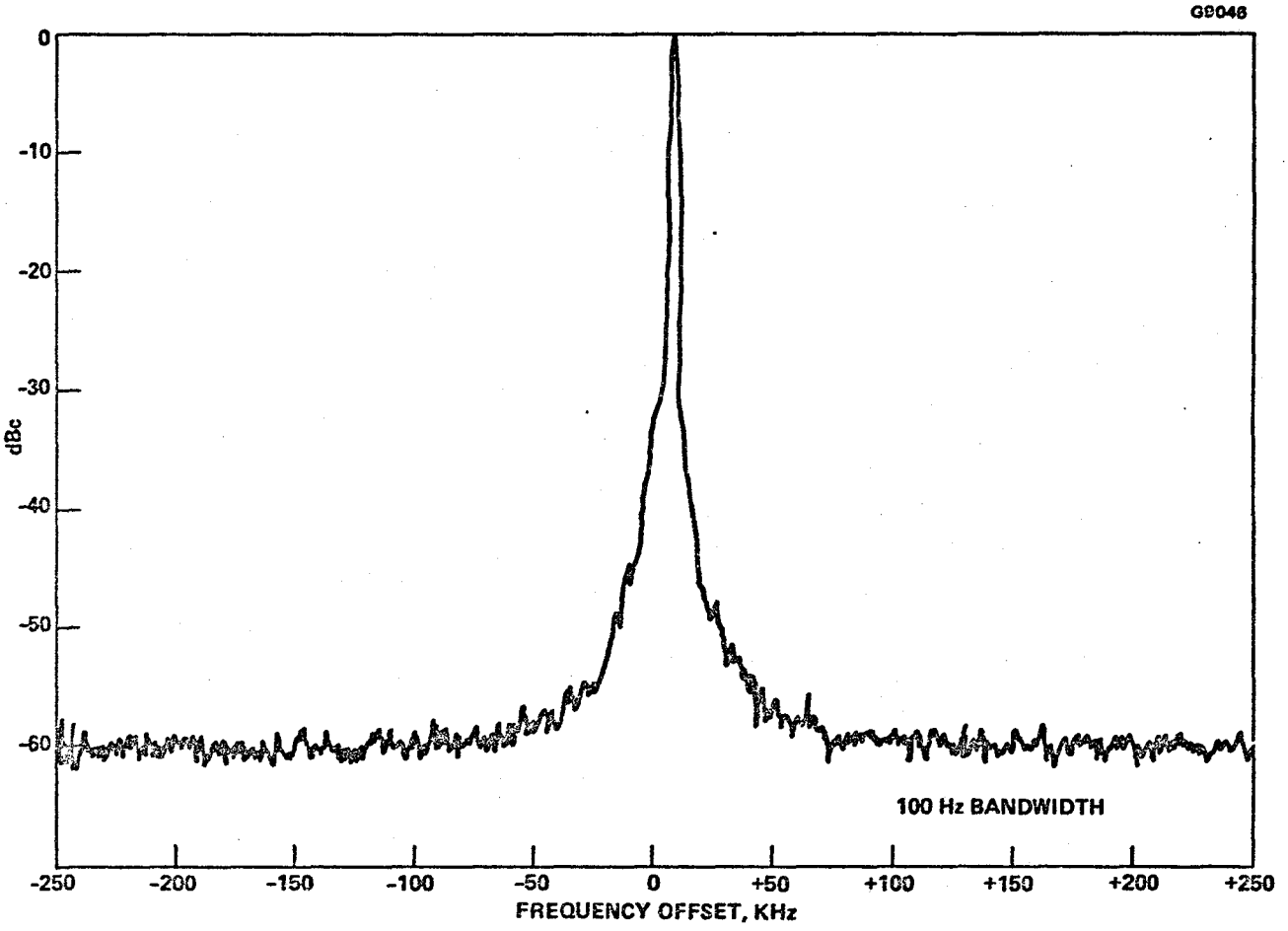


Figure 4-52 Output spectrum of 25 GHz FET oscillator.

$$\Delta\phi_{RMS} = \sqrt{2\int_{f_1}^{f_2} \mathscr{L}(f_m)df_m} \qquad (4.4\text{-}3)$$

Assuming that the dominate noise process has a 1/f FM noise distribution over the bandwidth of interest (10 kHz to 100 kHz for our case), the resulting $\mathscr{L}(f_m)$ has a $1/f^3$ dependence. Translating the above phase noise measurements into $\Delta\phi RMS$, based on the above assumptions, results in an oscillator phase noise of 7.2^o RMS over a bandwidth of 10 kHz to 100 kHz. Comparing this result with the 2^o RMS design goal indicates that work needs to be done to improve the oscillator phase noise.

The oscillator Q was measured by an injection locking technique utilizing the locking formula

$$Q_L = \frac{2f_o}{\Delta f_L}\sqrt{\frac{1}{P_C/P_S - 1}} \qquad (4.4\text{-}4)$$

where Δf_L is the total locking bandwidth, P_C the carrier power and P_S is the synchronizing power. The loaded Q determined with this technique was 350. A photograph of a completed oscillator mounted in a test fixture is shown in Figure 4-53.

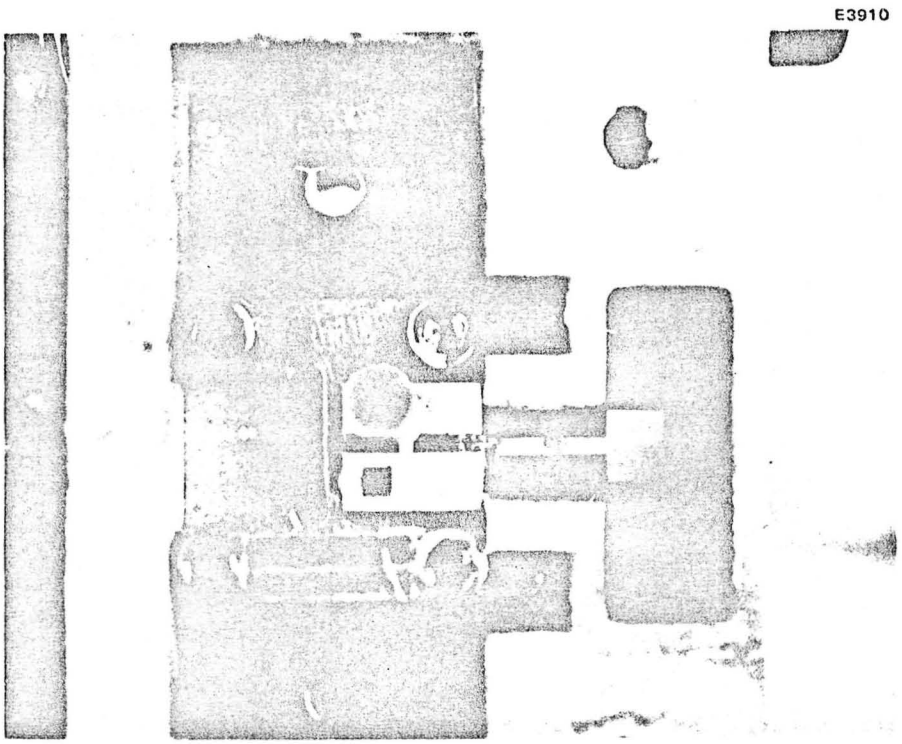


Figure 4-53 Photograph of completed 25 GHz FET oscillator.

5.0 LOW NOISE RECEIVER DEVELOPMENT

5.1 GENERAL CONSIDERATIONS

In this section the design and performance of the breadboard receiver (BR) and improved receiver (IR) will be discussed. The basic components of a receiver are a low noise amplifier, mixer and local oscillator. This program was primarily concerned with the development of these key components. Utilizing the best low noise amplifiers, a dual-gate FET mixer and FET local oscillator, a breadboard and improved receiver were to be constructed and evaluated for noise and gain performance.

Our fundamental design philosophy emphasizes the design, test and optimization of the key components as separate units. This approach allowed the determination and optimization of the parameters associated with each component which would maximize overall performance. Other advantages include:

- Simplified construction.
- Replacement of inferior or failed stages.
- Flexibility in final receiver configuration.

5.2 BREADBOARD RECEIVER

A block diagram of the breadboard receiver (BR) is shown in Figure 5-1. This receiver contains a minimum implementation of key components. The waveguide-to-microstrip transitions were removed from the test fixtures of each optimized component. Where appropriate, interstage blocking capacitors were added and the test fixtures were then cascaded together. The photograph in Figure 5-2 is a mockup of the BR to illustrate the method of implementation.

Initial tests were conducted with each component biased from separate power supplies. After the initial evaluation, the components were connected to a common supply buss through simple resistive networks with adjustable potentiometers. This network was mounted on the bottom side of the unit. The bias point of each stage was set to achieve optimum receiver conversion performance. The supply voltages required were +6.0 volts at 0.114 ampere and -4.0 volts.

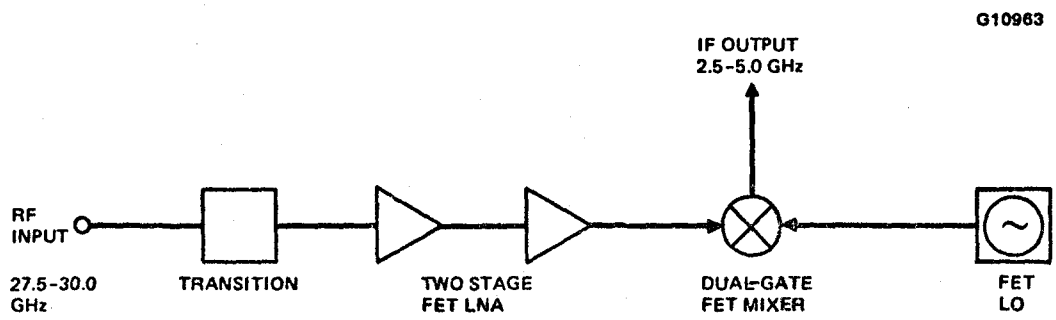


Figure 5-1 Block diagram of breadboard receiver.

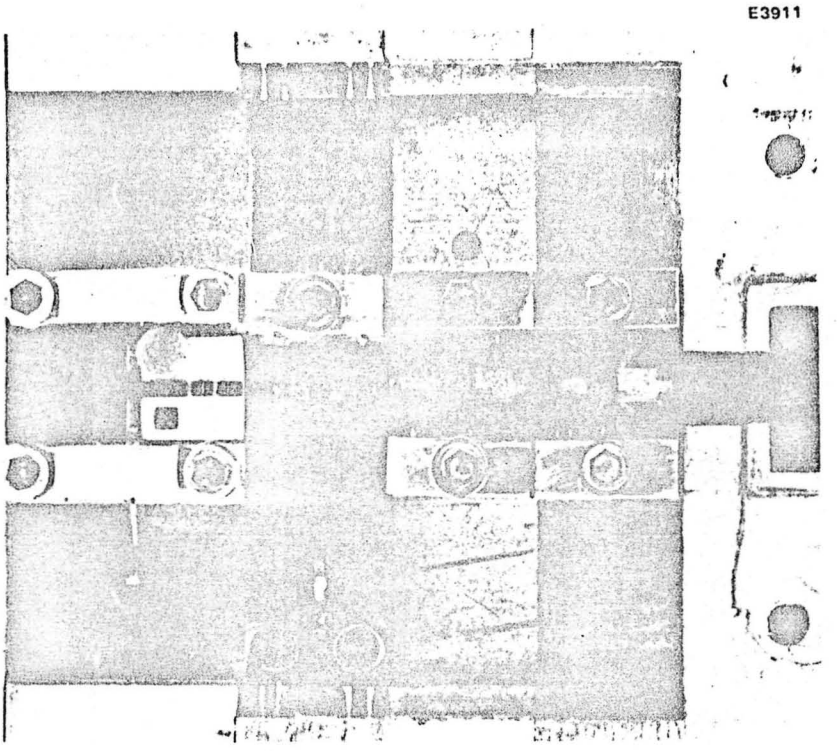


Figure 5-2 Mockup of the breadboard receiver.

The frequency performance of the BR is shown in Figure 5-3. At band center the conversion gain is 5.1 dB. Maximum conversion gain, 9.2 dB, was achieved at 29.0 GHz. Based on component performance, the noise figure was estimated to be 9 dB. Due to instrumentation problems, we were unable to measure the noise performance. The BR shown in Figure 5-4 with part of the top cover removed is 1.6 inches long and 1.5 inches wide. The overall receiver and component performance is summarized in Table 5-1.

5.3 IMPROVED RECEIVER

A block diagram of the improved receiver (IR) is shown in Figure 5-5. This receiver consists of an isolator, preamplifier, bandpass filter, mixer and local oscillator. Except for the isolator, the performance of the individual components has already been discussed.

5.3.1 Improved Receiver Description

The completed receiver is shown in Figure 5-6 with the top cover removed and Figure 5-7 shows the waveguide input, coaxial output and the bias network chamber. The IR requires a bias of +9.0 volts at 0.140 ampere and -8.0 volts; both voltages are internally regulated. The total power consumption of the unit is 1.26 watts. Schematics of the simple gate and drain bias networks are shown in Figure 5-8a. The positive voltage is regulated at 5.0 V and the negative voltage regulated at -2.5 volts.

The main body and mixer carrier form a coaxial air line with an 0.020 inch center conductor extending from the 0.085 inch coax which was used for the IF output port. An 0.020 inch gold ribbon was welded between the mixer IF microstrip circuit and the center conductor. The details of the transition and coaxial output are outlined in the cutaway illustration in Figure 5-8b. Evaluation of the transition using a microstrip load indicated that the transition achieved a 20 dB return loss from 2 to 8 GHz.

The waveguide isolator is a Hughes model 45141H-2000 low loss three port terminated junction circulator, shown in the photograph of Figure 5-9. The unit was optimized for the 27.5 to 30.0 GHz frequency band during construction. The

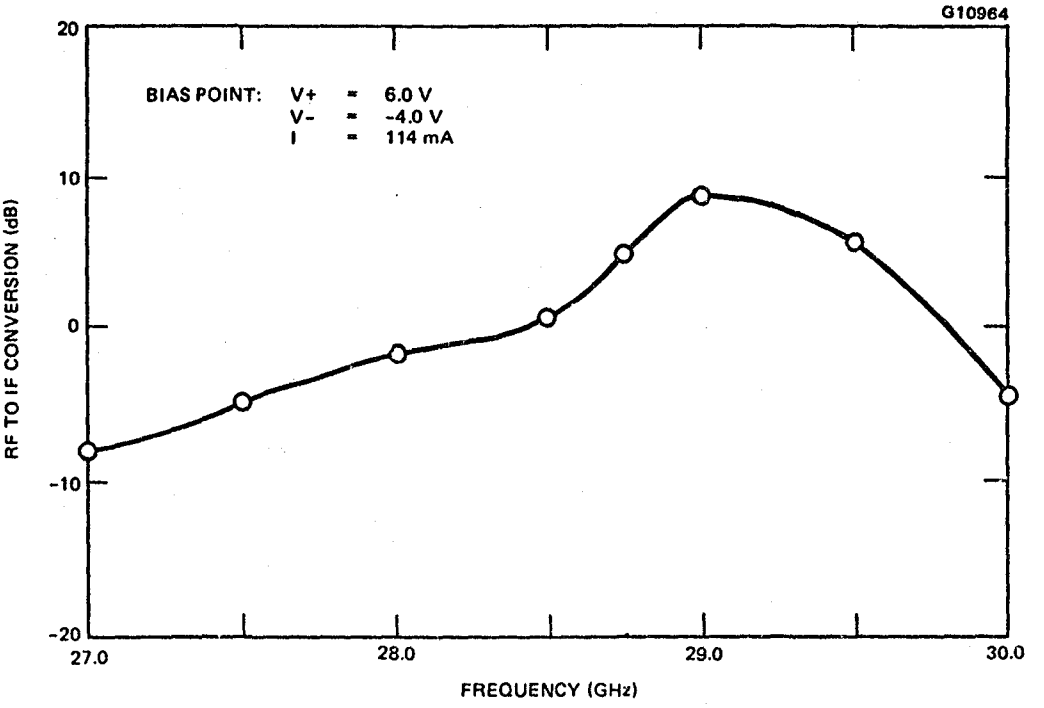


Figure 5-3 Frequency response of 30 GHz breadboard receiver.

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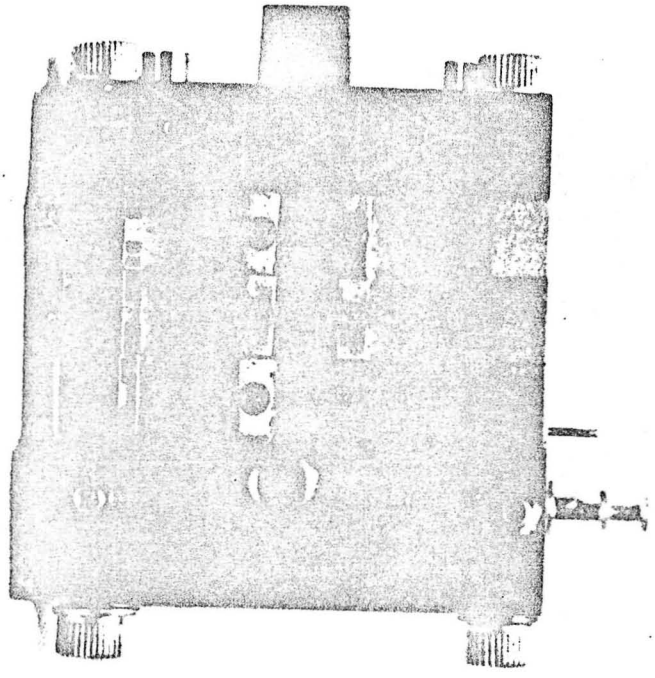


Figure 5-4 Completed breadboard receiver.

TABLE 5-1

BREADBOARD FET RECEIVER PERFORMANCE

Basic Receiver Performance	
Frequency of operation (3 dB)	28.7-29.6 GHz
Noise Figure (typ)	9 dB
Conversion Gain (29 GHz)	9 dB
Input Connector	WG
IF Output Connector	SMA Female
GaAs FET Low Noise Preamplifier	
Frequency of operation	27.5-30 GHz
Gain	9.4 dB
Noise Figure	7 dB
Dual-Gate FET Mixer	
RF Frequency (3 dB)	27.6-29.9 GHz
LO Frequency	25 GHz
IF Frequency	2.6-4.9 GHz
Conversion Loss	7 dB
Noise Figure	~13 dB
Local Oscillator	
LO Frequency	25 GHz
Output Power (typ)	10 dBm
Frequency Drift	0.18 MHz/^{o}C
Phase noise	7.2^{o} RMS integrated from 10 kHz to 100 kHz from the carrier

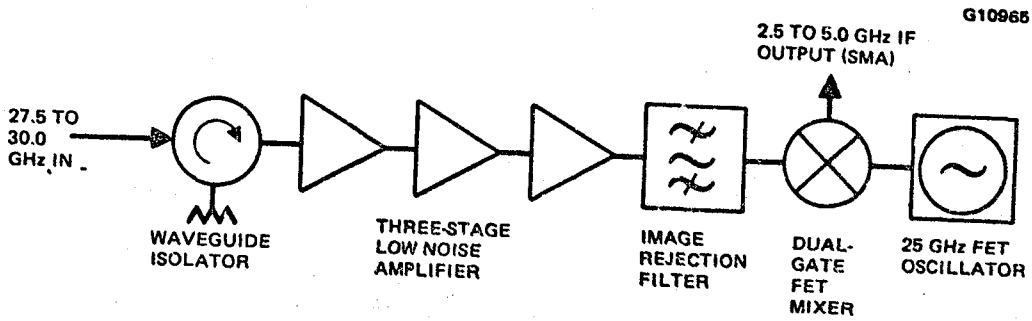


Figure 5-5 Block diagram of the improved FET receiver.

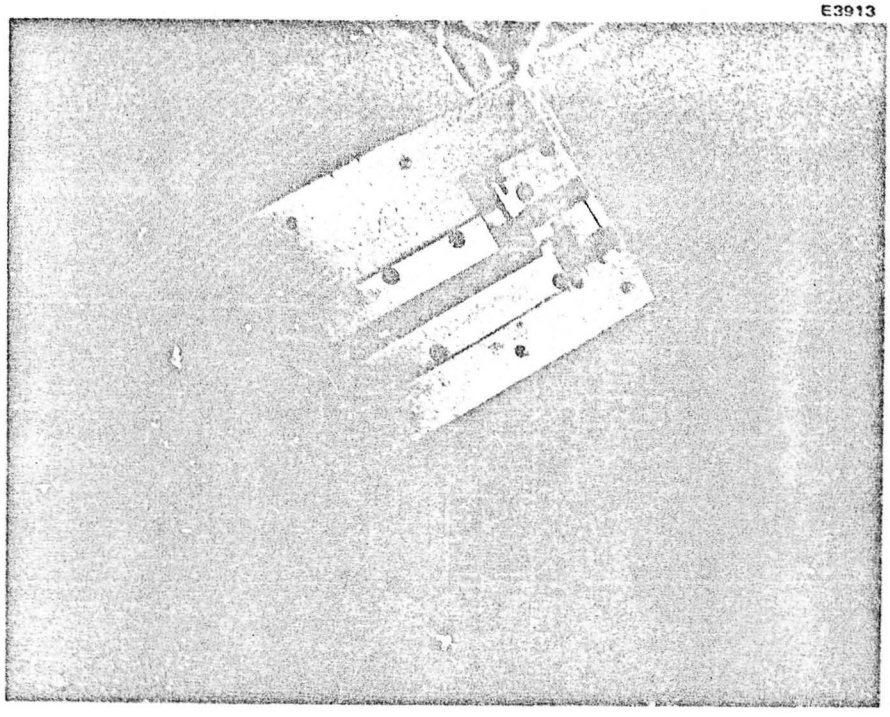


Figure 5-6 FET receiver (top view).

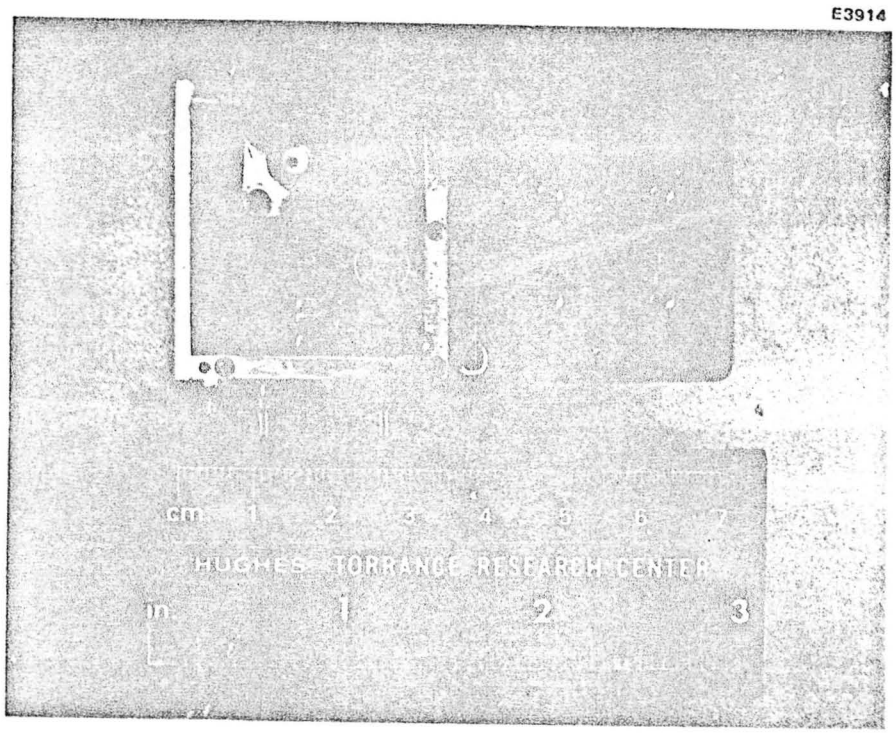
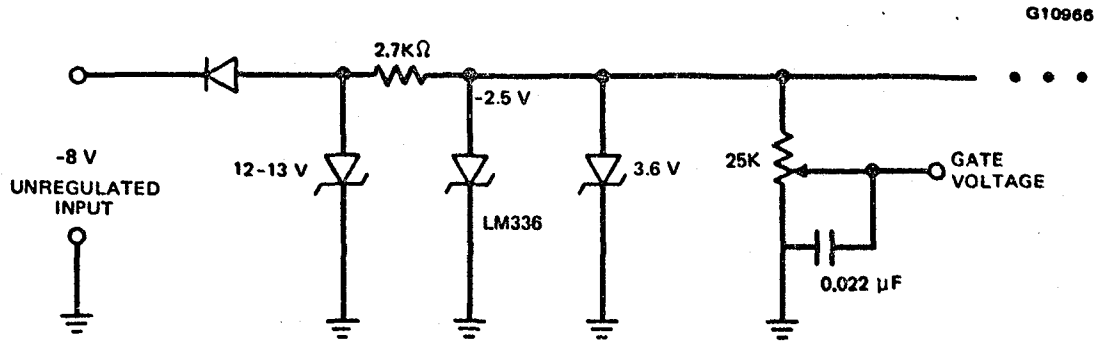
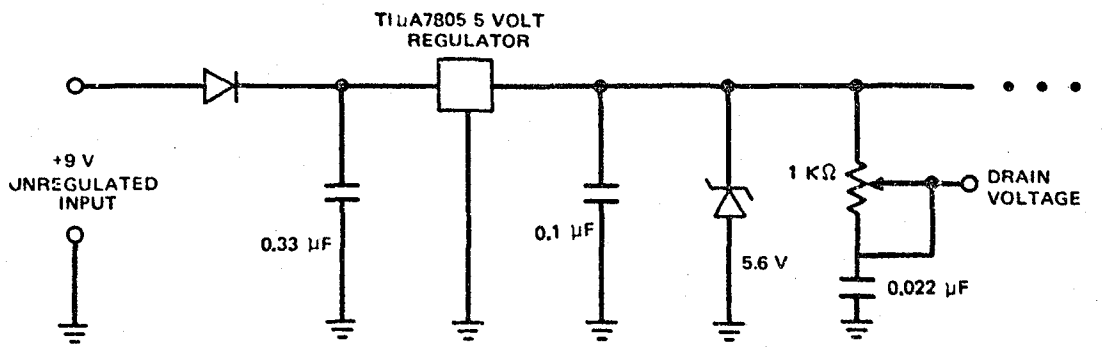


Figure 5-7 FET receiver (bottom view).



(a) REGULATED GATE BIAS NETWORK



(b) REGULATED DRAIN BIAS NETWORK

Figure 5-8a Schematic of regulated DC bias networks.

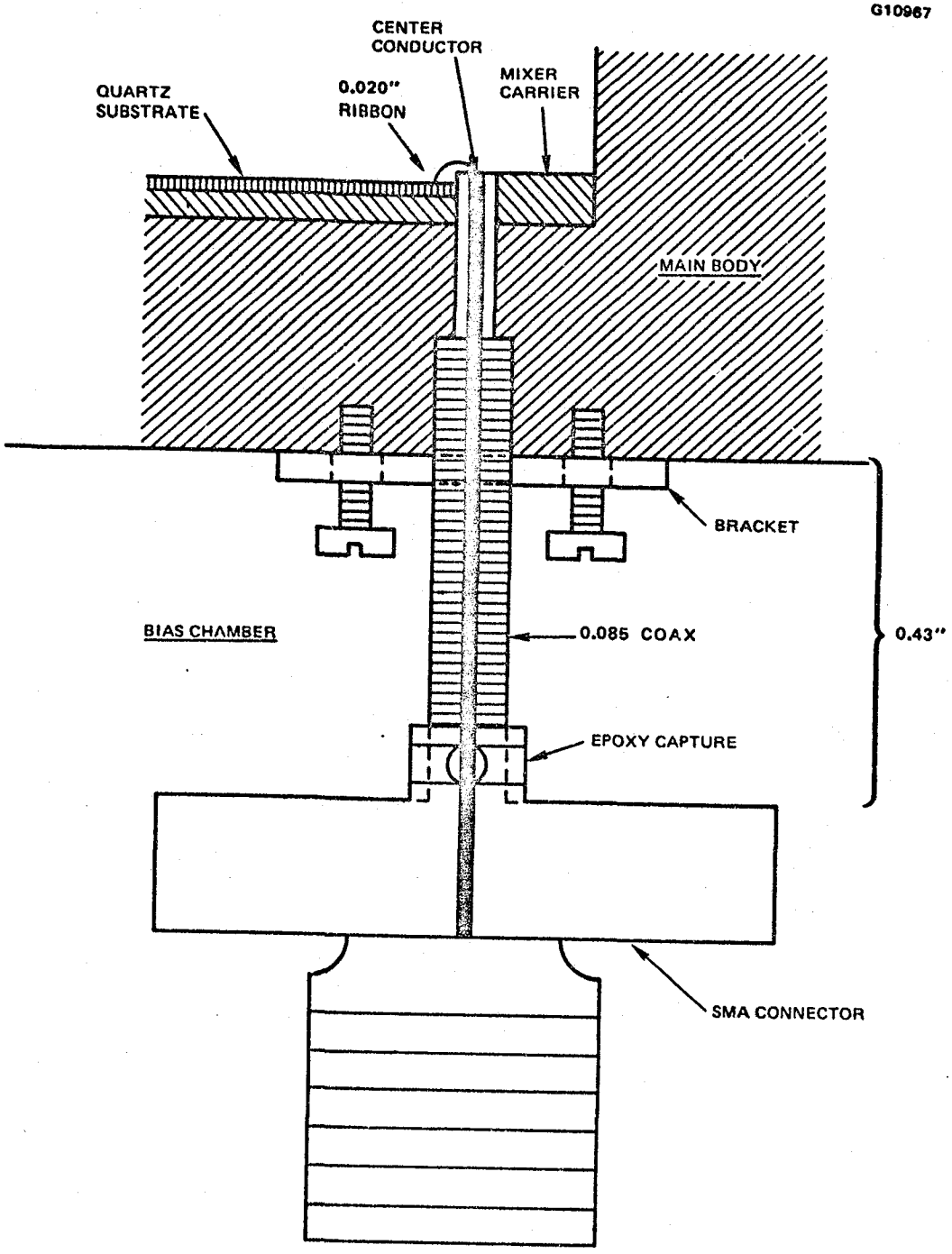


Figure 5-8b Cutaway view of IF transition and output port.

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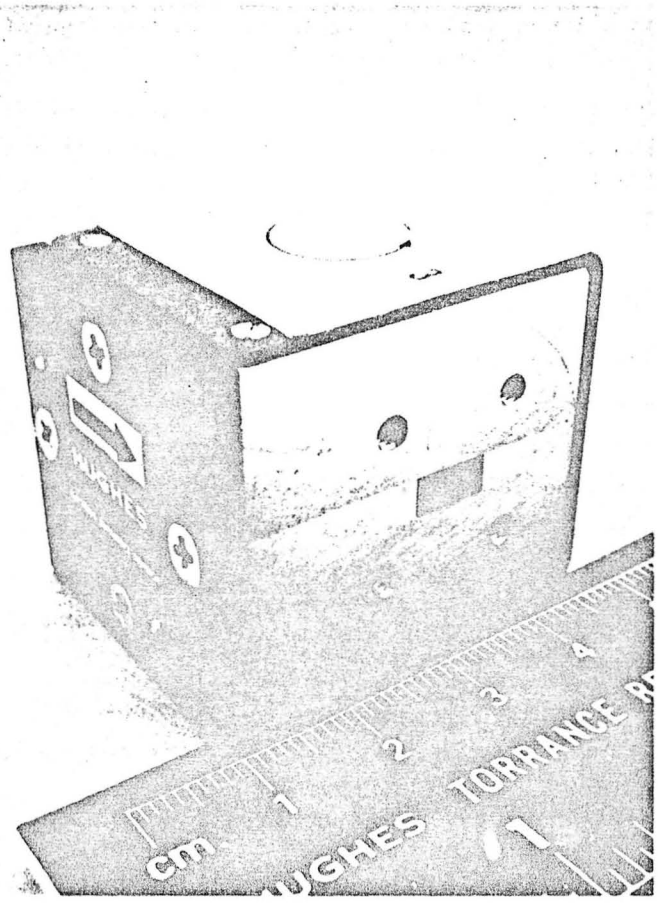

Figure 5-9 Ka-band waveguide isolator.

frequency performance of this isolator is shown in Figure 5-10. At band center the insertion loss measured a very low 0.25 dB and increased to 0.6 to 0.8 dB at the band edges. The return loss was 20 dB at 28.75 GHz and greater than 15 dB over most of the band. Isolation was >20 dB over the band. The in-line tee configuration allowed a clean, simple receiver configuration and was easy to interface.

Photographs of the completed IR are shown in Figures 5-11 and 5-12. The screw on the top cover allows fine control of the 25 GHz local oscillator frequency. The overall dimensions of the unit are 1.5x1.8x2.7 inches.

5.3.2 Improved Receiver Performance

The initial frequency performance of the IR is shown in Figure 5-13. At band center the noise figure is 4.6 dB with 17.4 dB associated conversion gain. The output power at the 1 dB gain compression point was -3.5 dBm. The IF mixer matching network was reoptimized for wider bandwidth. The frequency performance of the optimized receiver is shown in Figure 5-14. The conversion gain, 11.2 dB at 27.5 GHz, reaches a peak of 17.3 dB at 29 GHz before falling to 10.2 dB at 30.0 GHz. The noise figure, 6.3 dB at 27.5 GHz, decreases to its minimum value, 4.6 dB at 28.75 GHz, and rises to 6.3 dB at 30.0 GHz. At band center, 28.75 GHz, the noise figure is 4.6 dB with 17 dB associated gain. The performance is listed in Table 5-2. The noise figure varies by 2 dB over the band and the gain by 7.1 dB. The isolator frequency characteristics contribute to the noise figure variation and the limited mixer IF bandwidth to the conversion gain variation. The gain compression characteristic is shown in Figure 5-15. The power output at the 1 dB compression point is -5 dBm.

The input return loss of the IR is shown in Figure 5-16, the same as the isolator. The return loss of the IF port is shown in Figure 5-17. This is basically a measure of the mixer IF frequency match provided by the very limited matching network. The response is peaked just above 4 GHz (29 GHz RF) and reflects the variation in frequency conversion performance demonstrated by the IR. The difference in the mixer mismatch loss ~6 dB accounts for that variation.

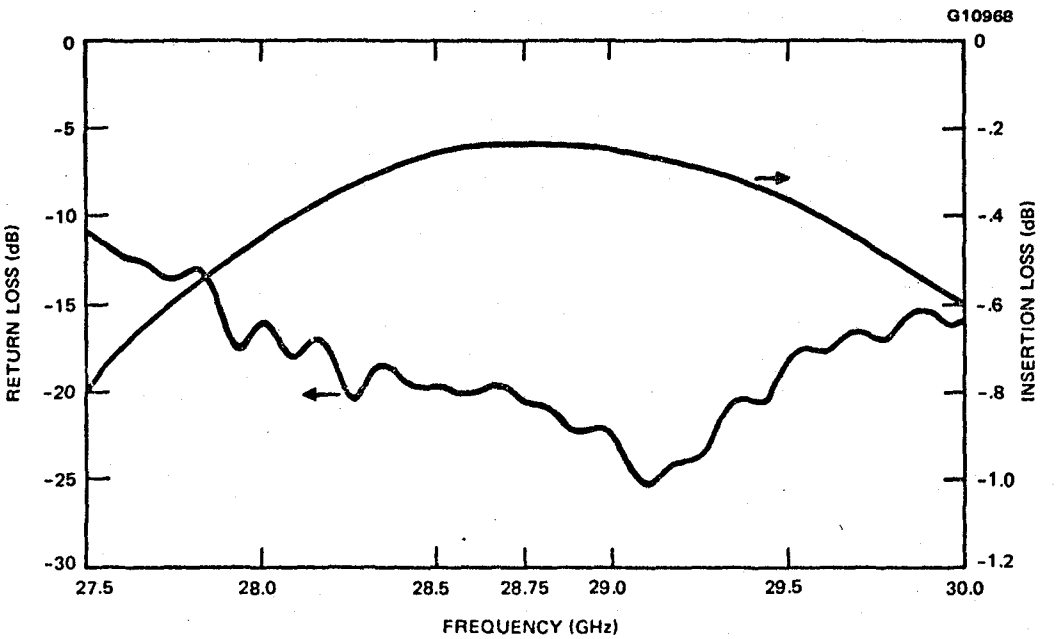

Figure 5-10 Performance of waveguide isolator.

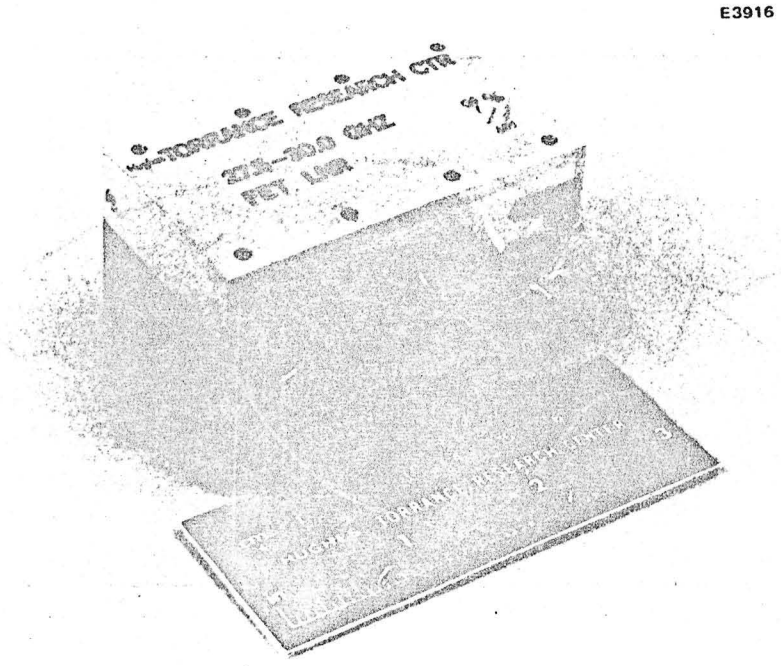

Figure 5-11 Completed receiver (top view).

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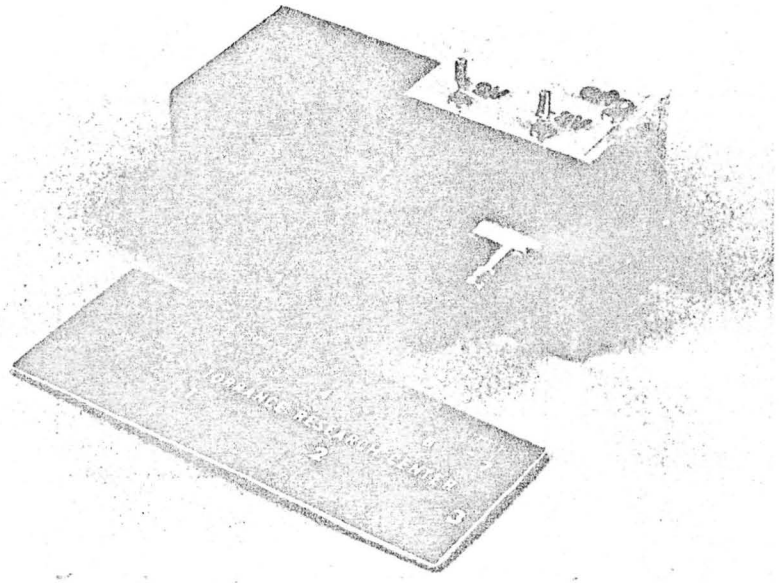


Figure 5-12 Completed receiver (bottom view).

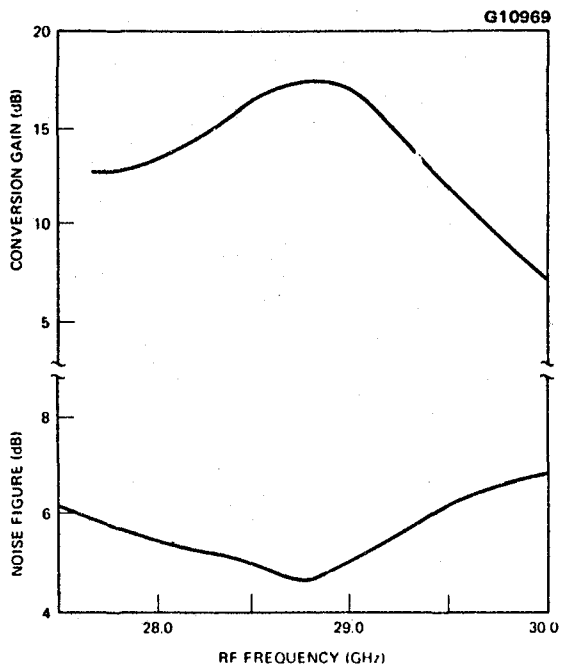


Figure 5-13 Initial frequency response of improved 30 GHz receiver.

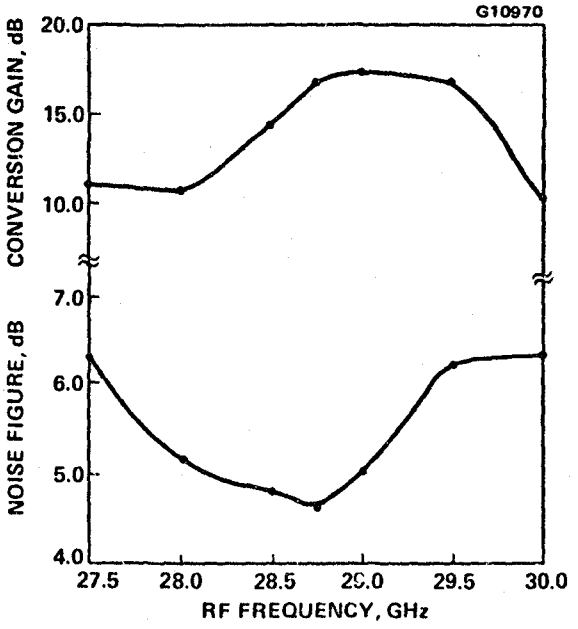


Figure 5-14 Optimized frequency response of improved 30 GHz receiver.

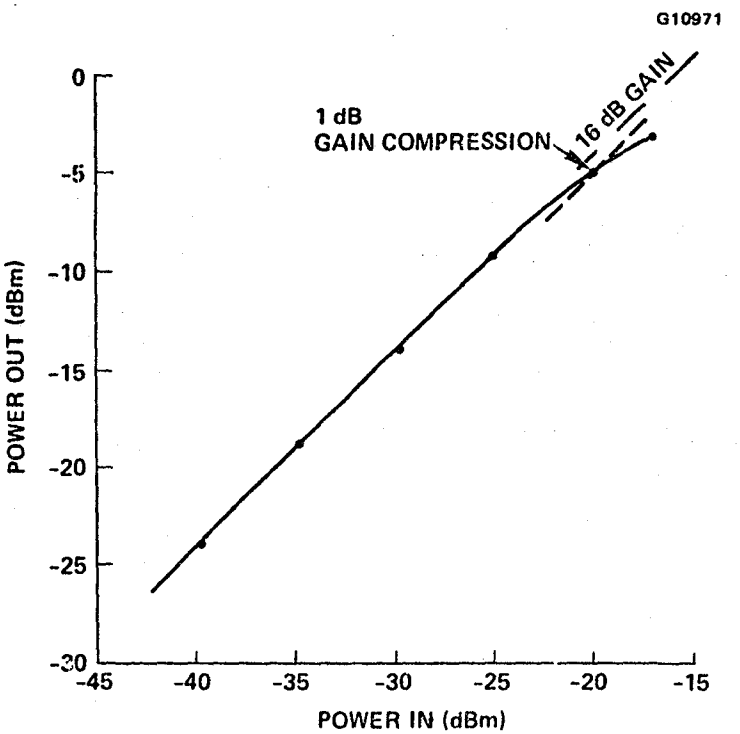


Figure 5-15 Gain compression characteristics of 30 GHz receiver.

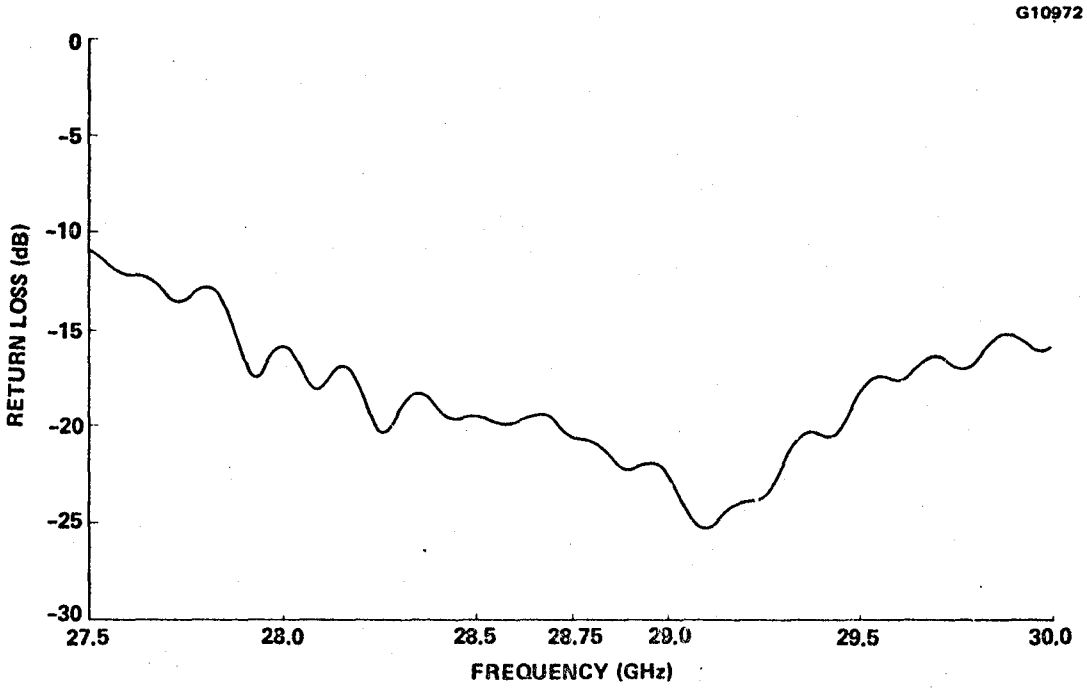


Figure 5-16 Input return loss of 30 GHz receiver.

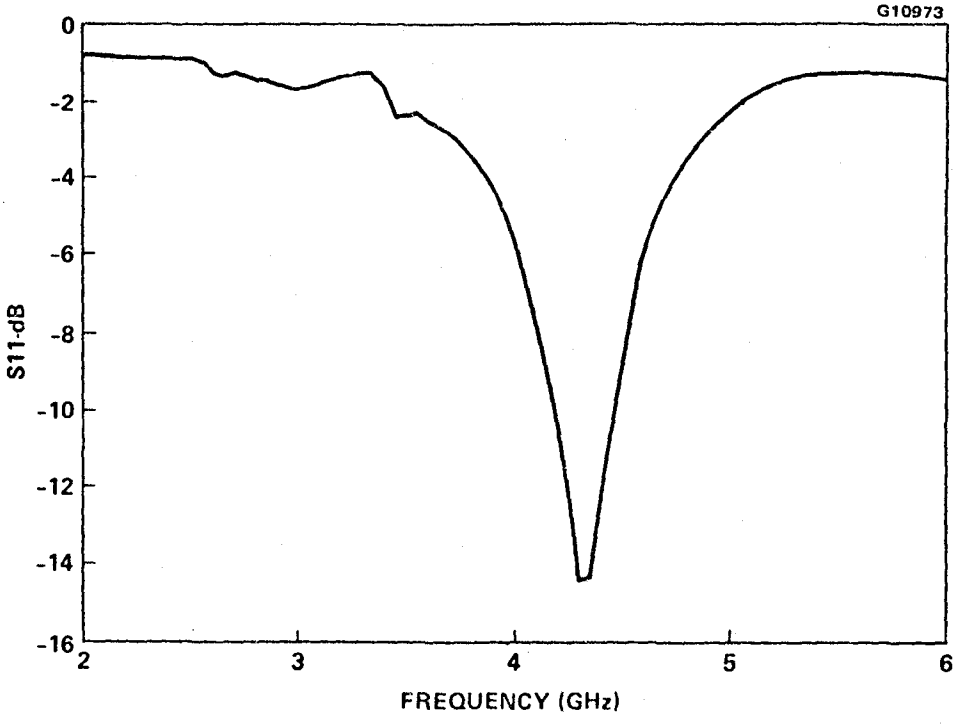


Figure 5-17 Output return loss of 30 GHz receiver.

C-3

TABLE 5-2

PERFORMANCE OF 30 GHz RECEIVER

Frequency GHz	Conversion Gain, dB	Noise Figure, dB
27.5	11.2	6.3
28.0	10.7	5.1
28.5	14.4	4.8
28.75	16.8	4.6
29.0	17.3	5.0
29.5	16.9	6.2
30.0	10.2	6.3

The RF to IF isolation of the IR measured -34 dB at 27.5 GHz, -46 dB at 28.75 GHz and -57.5 dB at 30.0 GHz. The LO isolation was -34.5 dB. The performance of the overall receiver and its components are summarized in Table 5-3.

5.4 SUMMARY

The breadboard receiver, our first attempt at integrating the various components, served as an excellent tool for diagnosing design and assembly problems and trade-offs. Most of the assembly problems were solved in the improved receiver.

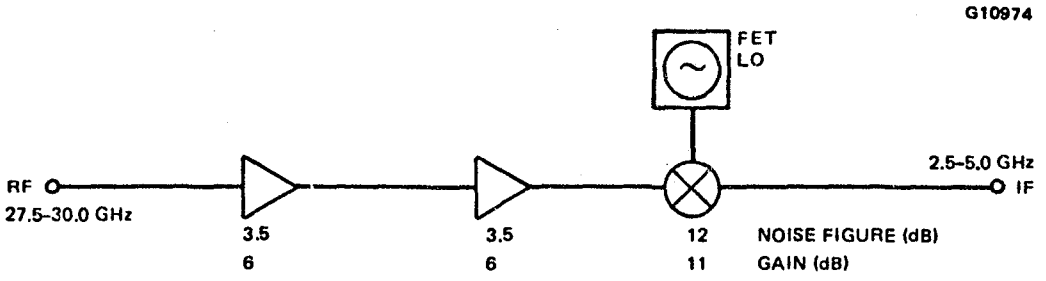
Table 5-4 highlights the major differences between the breadboard and improved receiver configurations. The IR includes an input isolator, an extra gain stage, an image rejection filter, and regulated, polarity protected bias circuitry absent from the BR unit.

Based on the program design goals for the individual components, it is possible to project the resultant receiver performance goals. The configuration, stage performance and overall receiver design performance goals are summarized in Figure 5-18. The estimated performance of the projected receiver is compared with

TABLE 5-3

IMPROVED FET RECEIVER PERFORMANCE

Basic Receiver Performance	
Frequency of operation	27.5 to 30.0 GHz
Noise Figure (typ)	5.5 ± 0.8 dB
Conversion Gain	14 ± 3.0 dB
Input Connector	WG
IF Output Connector	SMA Female
GaAs FET Low Noise Preamplifier	
Frequency of operation	26.5 to 30.5 GHz
Gain	20.0 ± 0.5 dB
Noise Figure	5.1 ± 0.7 dB
Dual-Gate FET Mixer	
RF Frequency	28.75 GHz
LO Frequency	25 GHz
IF Frequency	3.75 GHz
Conversion Loss	2.0 dB
Noise Figure	10.0 dB
Local Oscillator	
LO Frequency	25 GHz
Output Power (typ)	7.0 dBm
Frequency Drift	0.18 MHz/°C
Phase Noise	7.2° RMS integrated from 10 kHz to 100 kHz from the carrier
Input Isolator	
RF Frequency	27.5 to 30.0 GHz
Insertion Loss	0.4 ± 0.2 dB
Isolation	20 dB
Input Return Loss	-15 dB
Image Rejection Filter	
Passband	27.5 to 30.0 GHz
Insertion Loss	1.0 ± 0.3 dB
LO Rejection	15.0 dB
Image Rejection	25.0 ± 2.0 dB



FREQUENCY (GHz)	NOISE FIGURE (dB)	ASSOCIATED CONVERSION GAIN (dB)
27.5	7.2	20
28.75	5.4	23
30.0	7.2	20

Figure 5-18 Receiver performance design goal.

TABLE 5-4

COMPARISON OF IMPROVED AND BREADBOARD RECEIVER CONFIGURATIONS

Component	Improved	Breadboard
Input Isolator	Yes	No
Low Noise Amplifier	3 Stage	2 Stage
Image Rejection Filter	Yes	No
Mixer	Yes	Yes
Local Oscillator	Yes	Yes
Bias Network	Regulated	Unregulated

that of the BR and IR in Figure 5-19. The BR falls well below the design goal in both categories, as the result of the combined high noise figure amplifier and high conversion loss mixer. The improved receiver demonstrated vastly superior (3 to 4 dB) noise performance when compared to the breadboard and approximately a 1 dB lower noise figure than the design estimate. This is the result of a combination of lower noise, higher gain initial amplifier stages, and the addition of the third gain stage which raises the gain high enough to mask the mixer noise figure contribution.

The conversion gain of the improved receiver, though not achieving the performance level of the design estimate, is equally superior (10 to 15 dB) to the breadboard. It falls below that of the estimate primarily due to the difference between the projected and achieved mixer conversion gain, a difference that is somewhat offset by the additional gain in the LNA. The IR also includes components, the transition, filter, and isolator which increase the noise figure and reduce gain, that are not included in the design model.

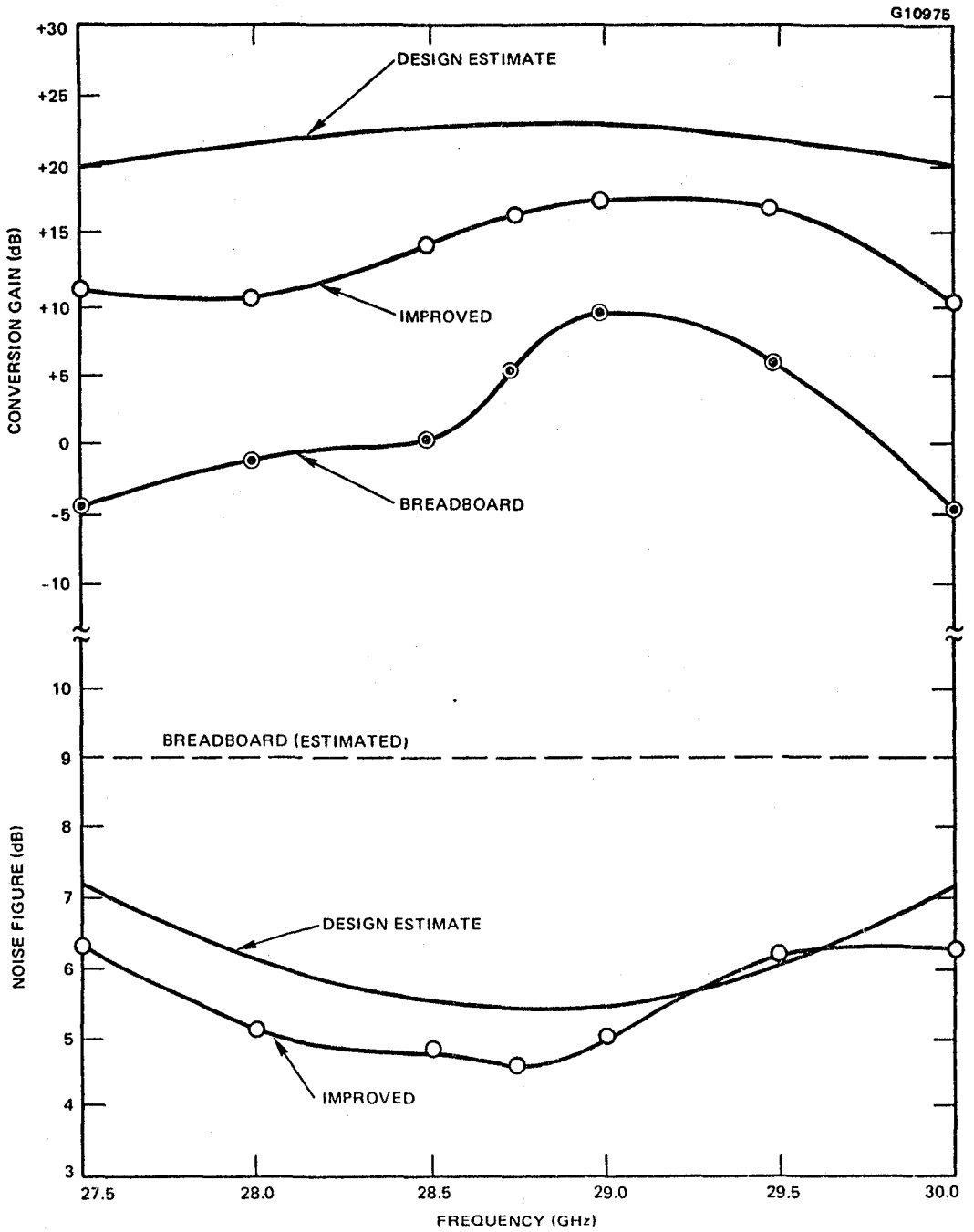


Figure 5-19 Performance comparison of the design estimate, breadboard and improved receivers.

6.0 CONCLUSIONS

A 30 GHz low noise receiver utilizing GaAs FET components exclusively has been demonstrated. This receiver has established new state-of-the-art performance levels and has thereby demonstrated the viability of FET technology at millimeter wave frequencies.

The key element in this successful effort was the 0.25 μm gate GaAs FET device. This device was fabricated with the aid of our advanced E-beam lithography system. It demonstrated a minimum noise figure of 3.3 dB at 29 GHz with an associated gain of 7.4 dB. The high associated gain in particular is significant. This device was primarily responsible for the receiver's state-of-the-art noise performance.

In addition to the device development, advances were made in FET based components at 30 GHz. These include a three-stage LNA with a 4.4 dB noise figure at 29 GHz, the first dual-gate FET mixer at 30 GHz and the first dielectric resonator stabilized FET oscillator at 25 GHz. However, to solidify FET technology for 30 GHz receiver applications, the following additional development is required:

- Low noise device and circuit development to further improve LNA noise figure and bandwidth.
- Dual-gate FET device and mixer circuit work to improve the mixer conversion gain and bandwidth.
- Device and GaAs materials work to improve the FET LO phase noise.

This combined materials, devices and circuits work would firmly establish FET technology in a leadership position at 30 GHz.

While this effort represents the initial thrust of FET technology into the millimeter wave region, it is currently competitive with the best diode based technology. The best reported result with a diode mixer/IF amplifier combination is a 5 dB double sideband noise figure at 30 GHz.[20] This was accomplished with

a narrow band IF amplifier at 30 MHz. Comparable wideband IF systems typically have a 2 dB higher noise figure. In contrast to diode technology, FET technology at this frequency is still in its infancy, and further significant progress is expected in the near term.

Projecting this technology into the very near future (approximately two years), we anticipate device noise figures to drop to 2.4 dB at 30 GHz. Such devices will result in FET based receivers with noise figures below 3 dB at 30 GHz and cooled units with a noise temperature below 120°K. A few years ago such projections would have seemed visionary; however, in view of our current results these projections appear realizable.

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APPENDIX A
RELIABILITY TEST

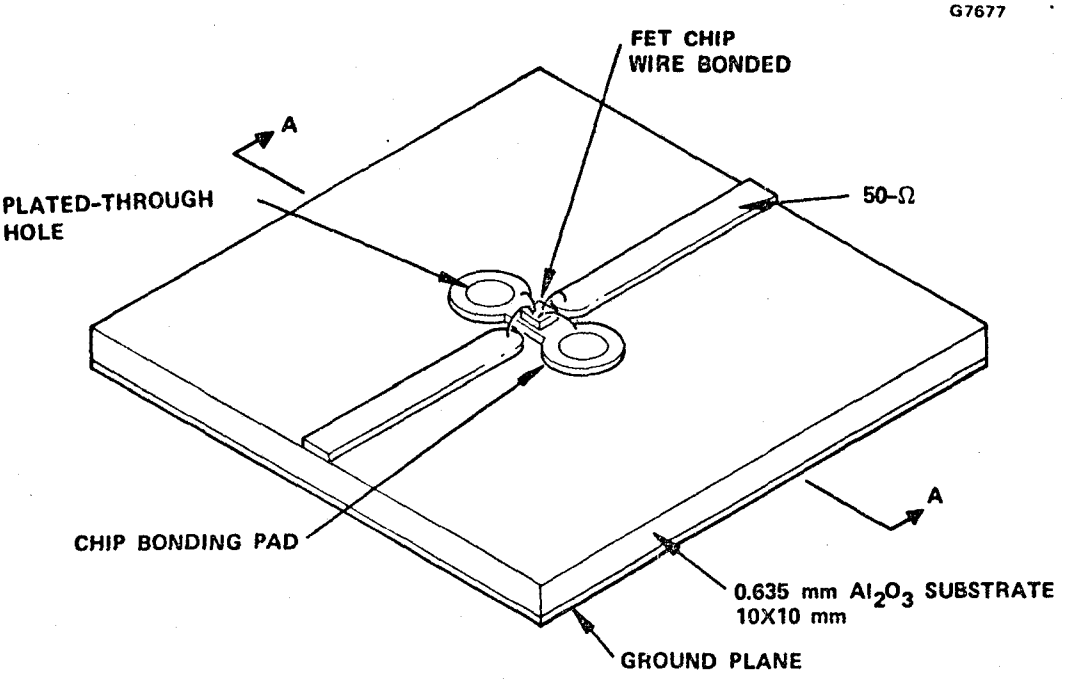
Part of the classical method for estimating the mean time to failure (MTTF) of FET devices at normal operating temperatures has been to subject them to accelerated life tests at elevated ambient temperatures. The aging characteristics and operational life span of FETs, biased and unbiased, can be determined in a relatively short period of time using this type of constant stress test. The goal of our test was to determine if the experimental FET devices developed for this program would exhibit lifetimes comparable to previous devices. This investigation was not intended to be a comprehensive study of device degradation, failure mechanisms or useful lifetime, but was intended to provide a "spot check" of our device processing techniques.

Test Approach

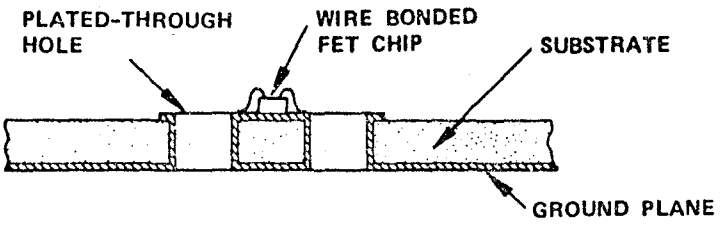
To characterize the reliability of the new device structures, 6 device samples were mounted on carriers as shown in Figure A-1 and Figure A-2. These carriers were selected to be compatible with previous tests and hardware. The devices were epoxied to the test carrier with silver epoxy and gold wire bonds attached to the source, gate and drain.

The devices were selected from the lot, SM03, which was fabricated with vapor phase epitaxial material using our standard metallization system. The device, shown in Figure A-3, was the 2 cell, "H" type 0.5x75 μm/cell configuration with drain currents at I_{DSS} (V_{GS} = 0) ranging from 5 to 31 mA.

The elevated temperature life tests were performed in bias ovens of a type originally developed by the Hughes Research Laboratories (HRL) for life testing semiconductor devices. Figure A-4 shows one of these ovens with its insulated cover removed. The heart of the oven consists of a stainless steel block that is heated along its full length by a cartridge heater. The GaAs FET chip test samples on their alumina microstrip carries were mounted in the chamber of the stainless steel block and covered by a quartz lid. To keep the chips clean and dry during operation, the oven chamber was continually purged with slowly flowing dry nitrogen derived from a liquid source.



(a) TOP VIEW.



(b) CROSS SECTION THROUGH CENTER PERPENDICULAR TO MICROSTRIP LINES.

Figure A-1 Microstrip chip carrier.

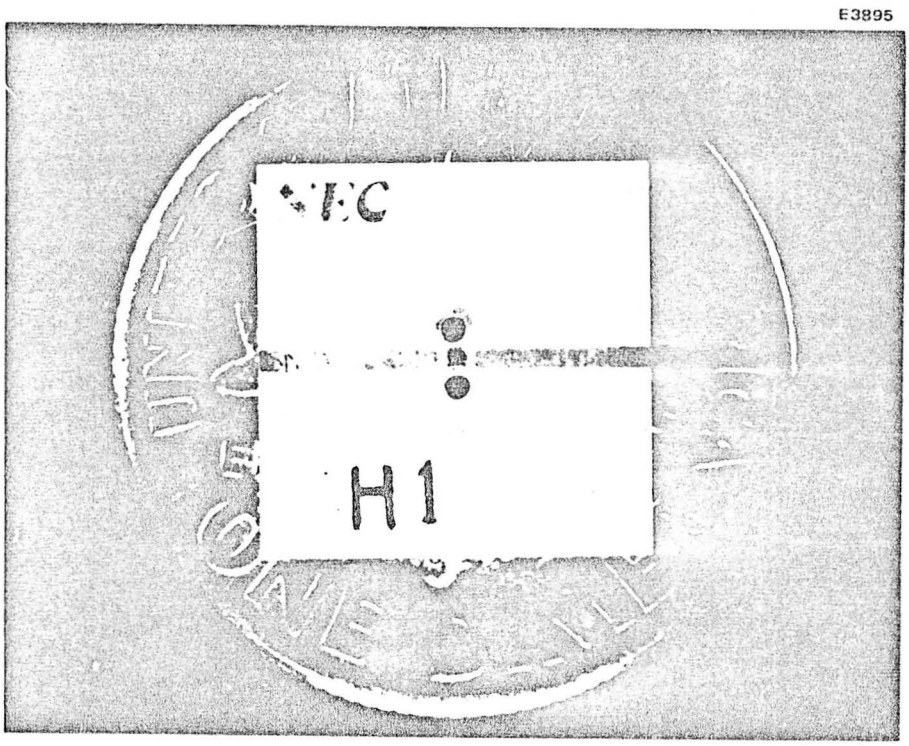


Figure A-2 FET mounted on test carrier.

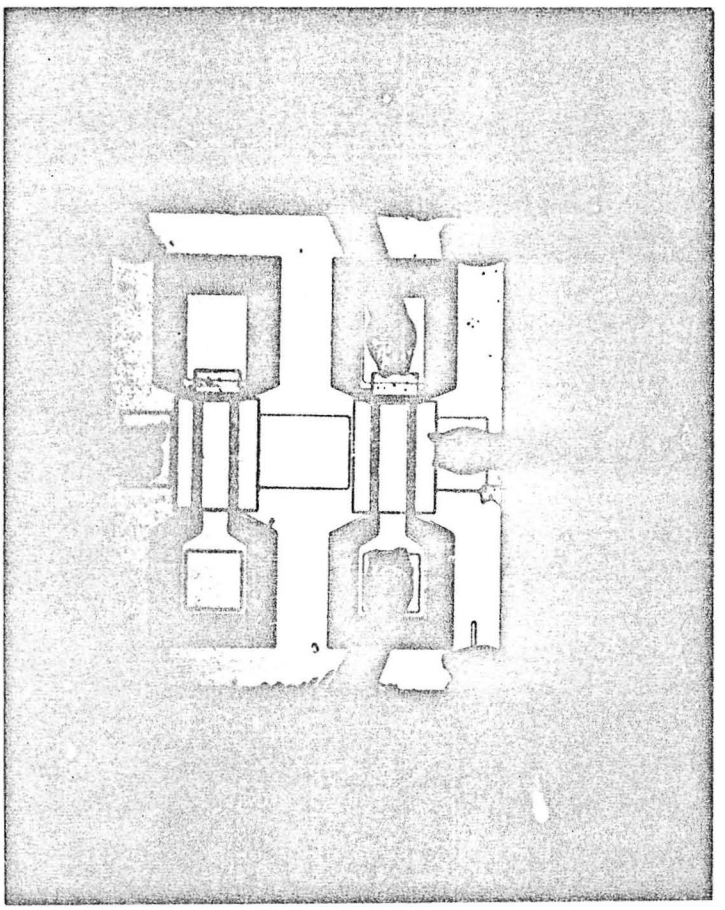


Figure A-3 "H" type SM100 device.

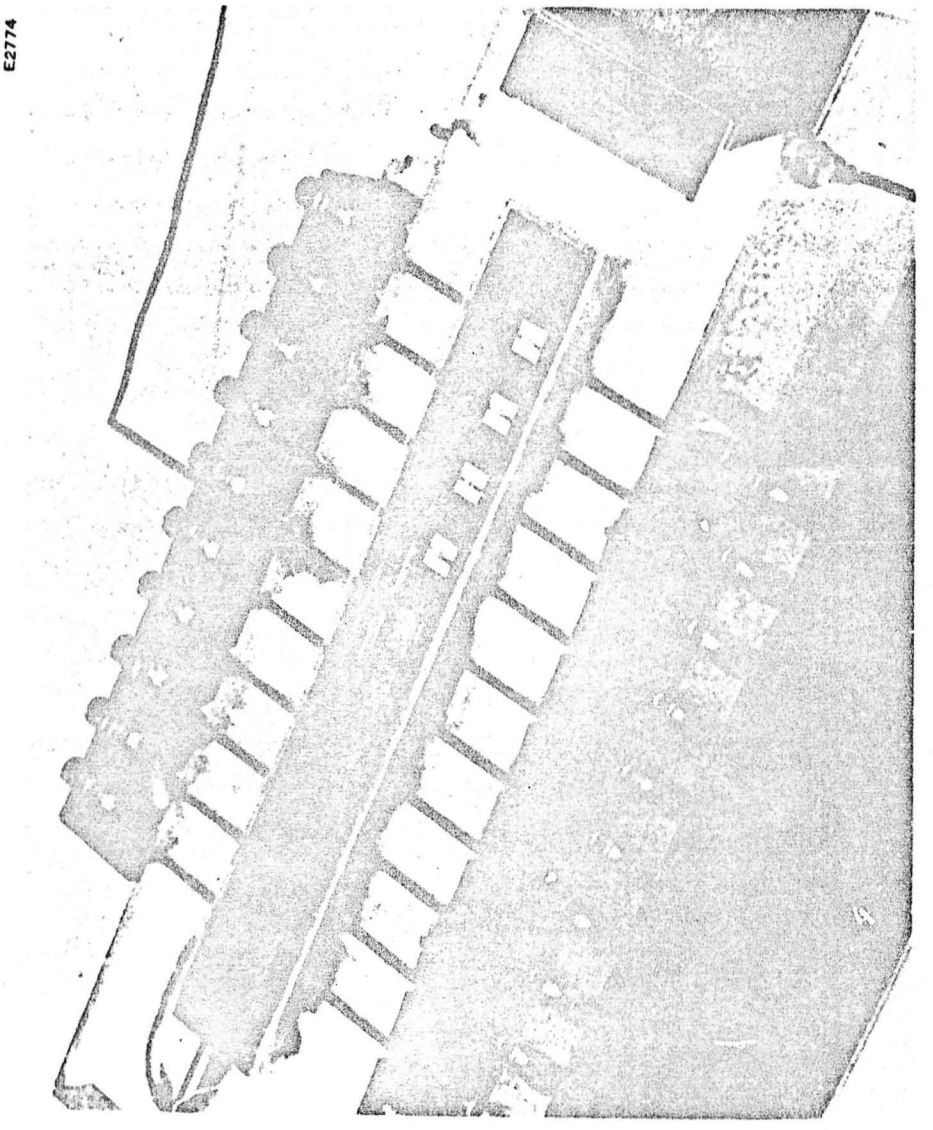


Figure A-4 HRL-developed bias oven with the insulated cover removed.

Gate and drain bias lines were brought into each sample position with 50-ohm coaxial transmission lines consisting of coaxial stainless steel, glass tubing and nickel wire. These coaxial lines extended through the insulated walls of the oven to the outside, where, at room temperature, the coaxial lines connected to gate and drain bias filters. These were essentially low-pass RC filters that acted to reduce any tendency of the biased FETs to oscillate. A schematic of the bias circuit for an oven is shown in Figure A-5. These tests were conducted at an oven temperature of 200°C. All the devices were biased at V_{DS} = 3.0 volts and I_{DSS}. Based on IR measurements, the channel temperature of these devices is estimated to be 10 to 20°C above ambient. However, due to the uncertainty in the actual channel temperature, the ambient temperature will be assumed in the following discussion.

Results

The test was conducted for approximately 4000 hours during which the drain current, I_{DSS}, of each sample was recorded periodically. The drain current versus the time at elevated temperature for each of the six devices is shown in Figures A-6 and A-7. None of these devices were subjected to a pretest burn-in, and some drain current variation early in the test was expected. However, the I_{DSS} of a few of the devices fluctuated wildly during the first 900 hours of the test. We believe that this is the result of device oscillations caused by long lines in the gate dc bias network. Approximately 900 hours into the test the gate of each device was dc grounded in the oven and the erratic behavior ceased.

Device failure criterion was selected to be a $\pm$10 percent change in I_{DSS} from the starting I_{DSS} (900 hours). This is indicated with the dashed lines marked "L" in Figures A-6 and A-7. Generally, the I_{DSS} of the devices varied by less than 10 percent during the life test period. The device which demonstrated more extreme variations also showed severe degradation as the test progressed and was considered failed at 3500 hours.

The small number of samples and limited data prevents a conclusive determination of the MTTF. Assuming a log-normal distribution, the failure at 3500 hours which represents 14 percent (1/N+1) cummulative failures can be used to estimate the

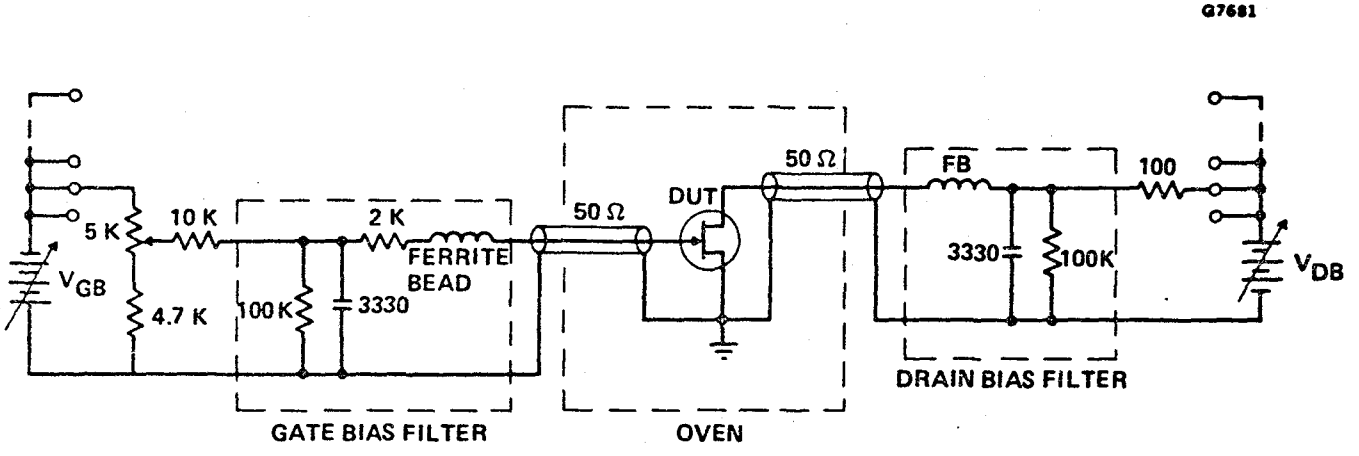


Figure A-5 Schematic of the bias circuits of the test oven.

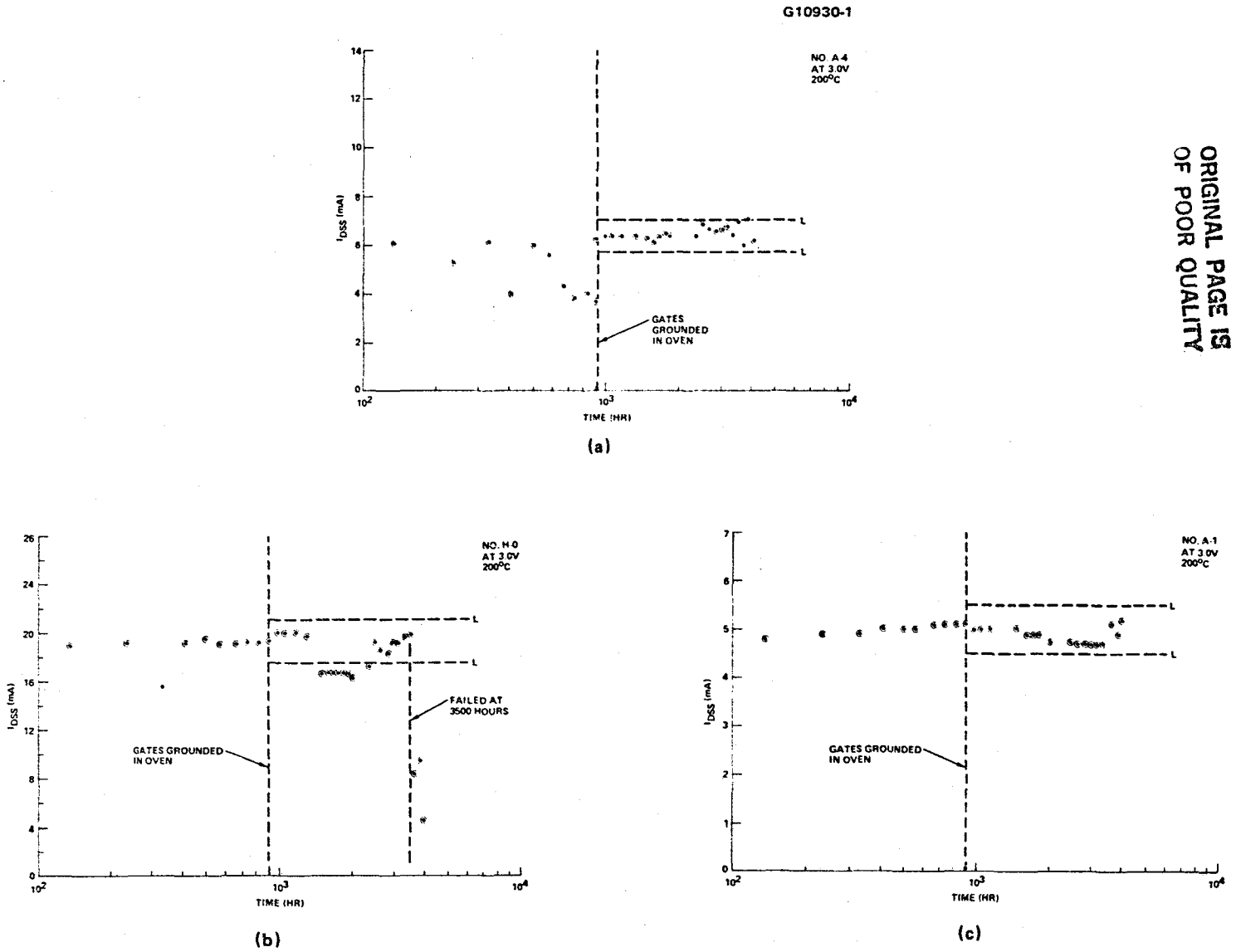


Figure A-6 I_{DSS} versus hours accumulated at 200°C.

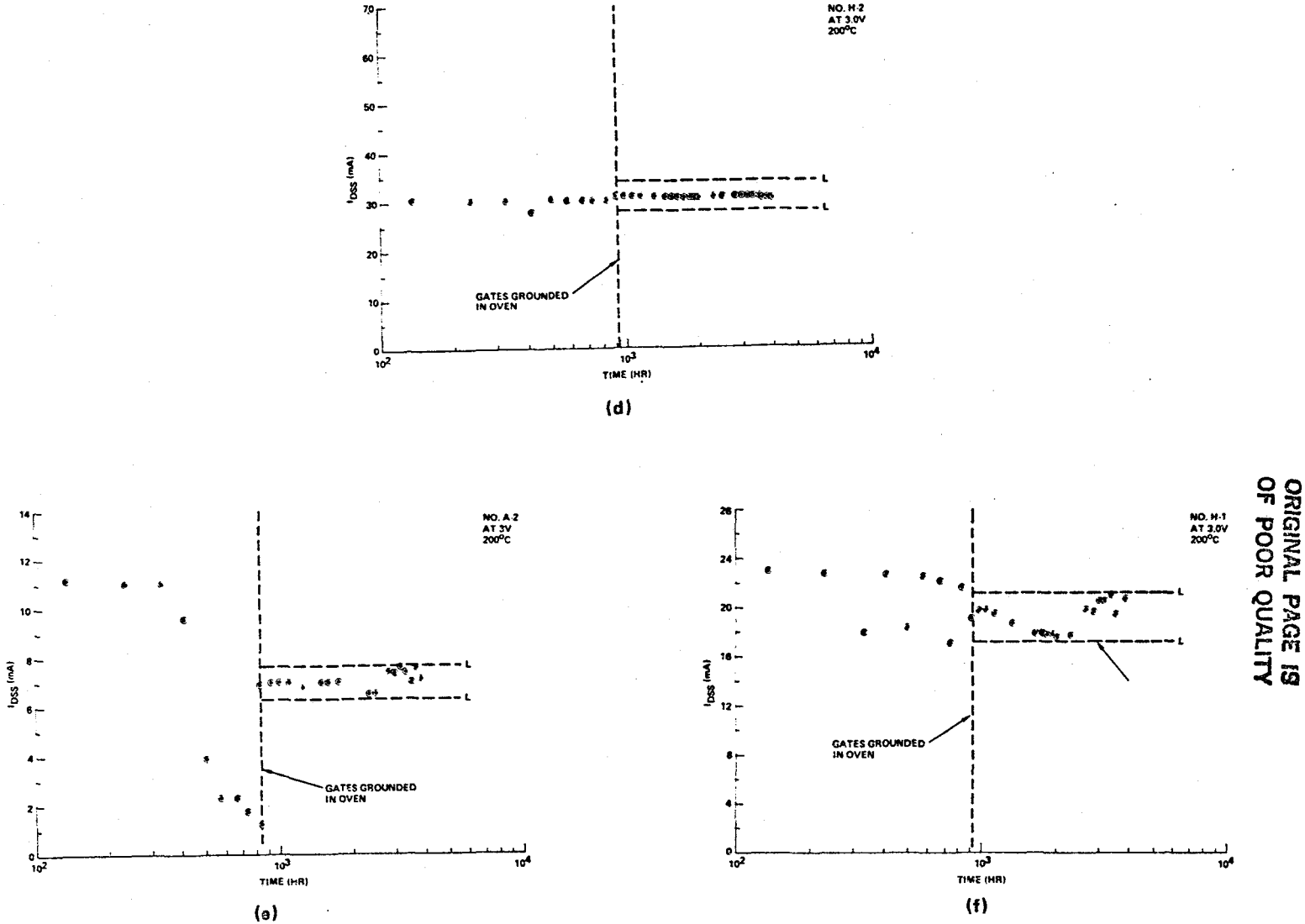


Figure A-7 I_{DSS} versus hours accumulated at 200°C.

median device life (50 percent failed) as shown in Figure A-8). An extrapolated median life of 5000 to 10,000 hours at 200°C is obtained if the shape parameter, σ, has a value between 0.2 and 1.0. This suggests that at elevated temperatures the experimental devices are comparable to other devices in operating life.

Using the ambient temperature an Arrhenius plot of some recent Hughes device results[21], a NEC unbiased FET result[22] and our current estimated result is shown in Figure A-9. The MTTF of the experimental devices at normal operating temperature is shown to be comparable to previous devices if the activation energy of the failure mechanism is similar to the other devices.

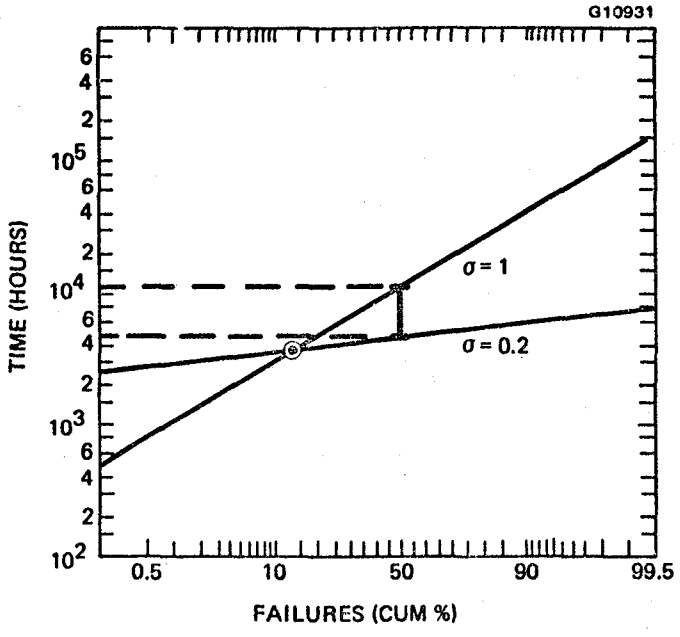


Figure A-8 Failure of biased experimental devices at 200°C ambient.

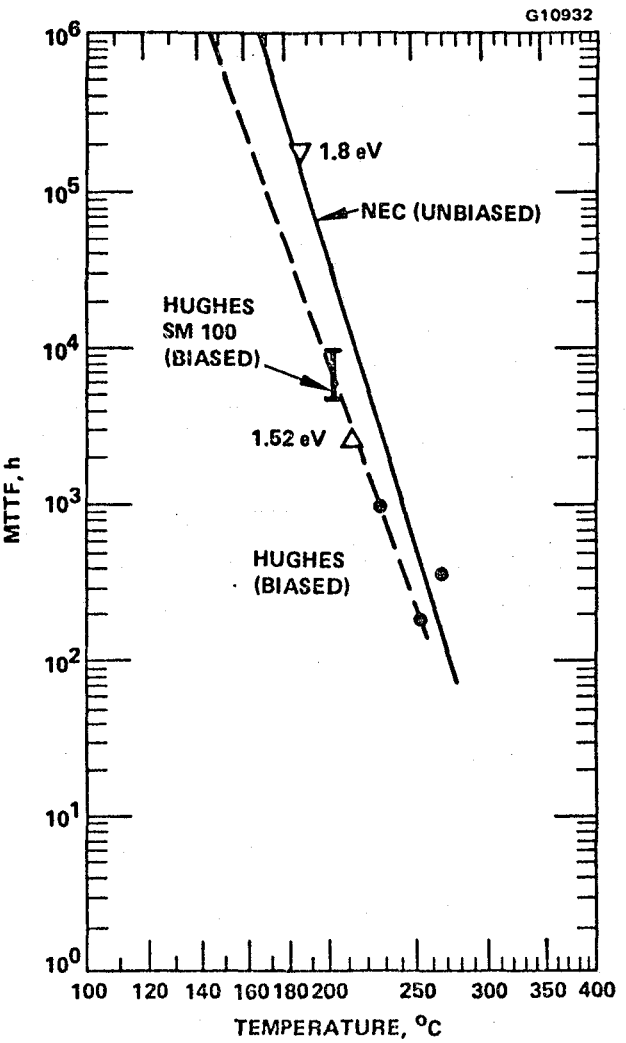


Figure A-9 MTTF as a function of ambient temperature.

APPENDIX B

FAILURE ANALYSIS OF DUAL-GATE FET LOT D5

During the mixer development a problem occurred in the D5 lot of devices. In an attempt to understand the problem, several SEMs were taken of the failed portions of the device. SEM photographs of a gate 1 to gate 2 failure, a gate 1 to source failure, and a gate 2 to drain failure are shown in Figures B-1, B-2, and B-3, respectively. The electrodes exhibit deformed areas where the gate material was molten and extruded through the gate oxide toward the other electrode. Craters have been formed in the GaAs material between the electrodes at these failure points. Measurements on the devices after failure indicate a current flowing through the damaged interelectrode area. We believe that these failures are the result of a high voltage arc over, possibly static, or a device defect resulting in breakdown.

An X-ray dispersive analysis of the device channel areas and chip surface was performed to determine if the burn out was the result of surface contamination by a foreign material. The results of the analysis are shown in Figures B-4 and B-5. No foreign substances were present in the channel area. On the external chip surface, silicon and silver were identified. The silicon, a particle that may have been left from a number of processes, was not a probable cause of failure. Silver paint was used to mount the device for the SEM and X-ray analysis. It was also used in tuning the mixer circuits, but extreme care was taken to ensure that the device was not contaminated. In addition, there was no evidence of silver in the channel area. The analysis suggests that surface contamination did not cause the device failures.

The evidence indicates that the failures are lot dependent. Only devices from D5 exhibited this failure mechanism. We believe the failures may be due to a material or processing problem unique to lot D5 which results in device deterioration eventually leading to catastrophic failure.

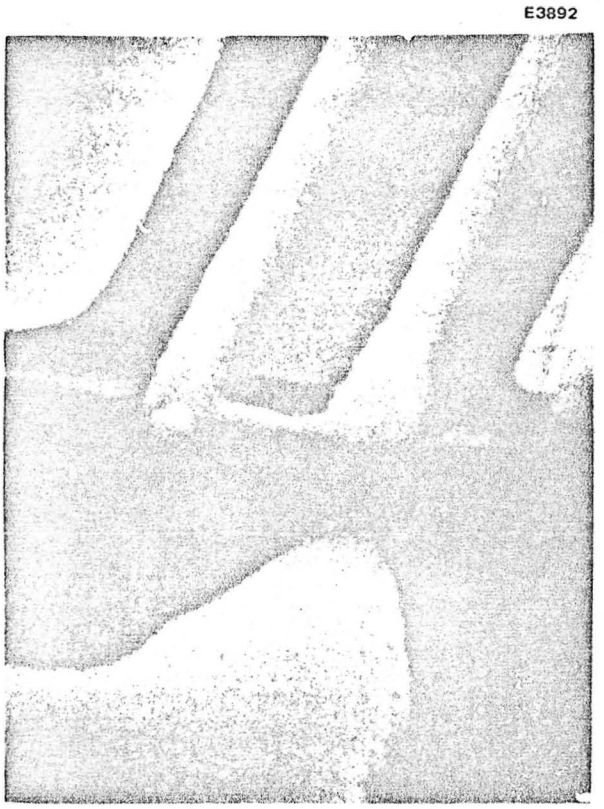


Figure B-1 SEM of gate 1 to gate 2 failure.

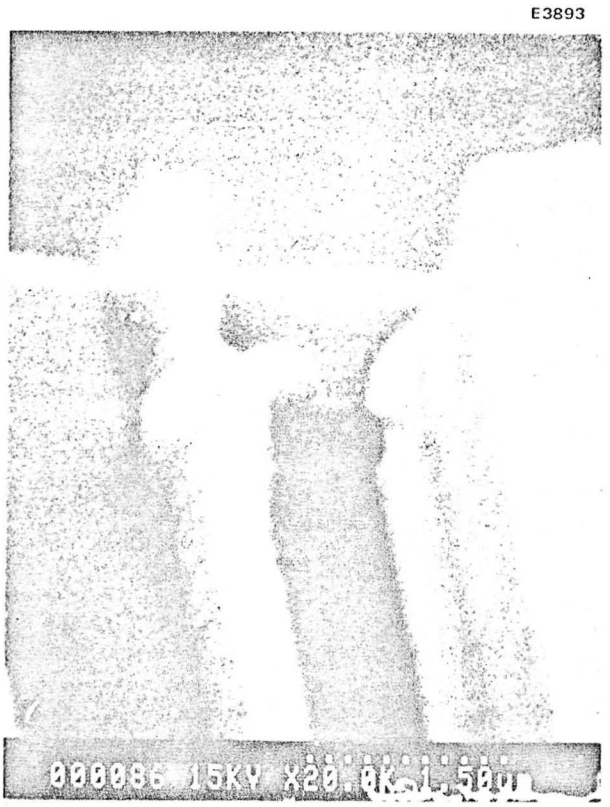


Figure B-2 SEM of gate 1 to source failure.

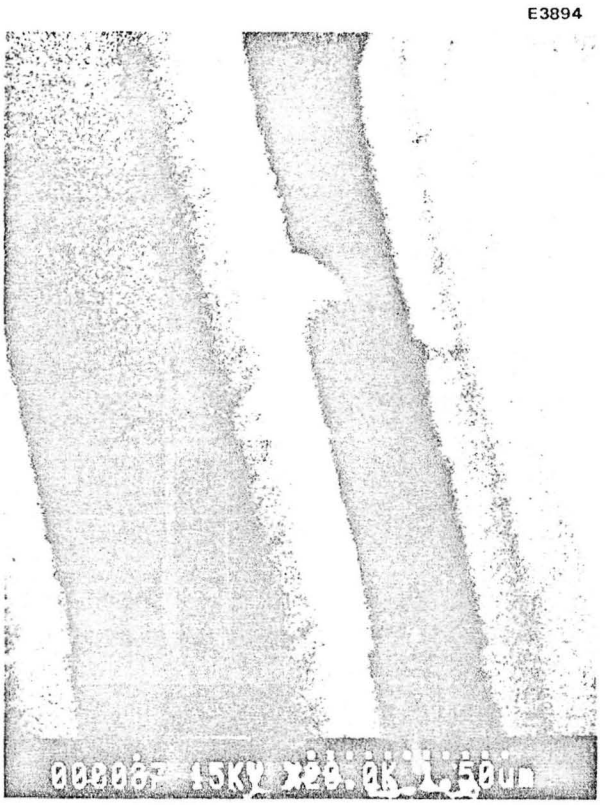


Figure B-3 SEM of gate 2 to drain failure.

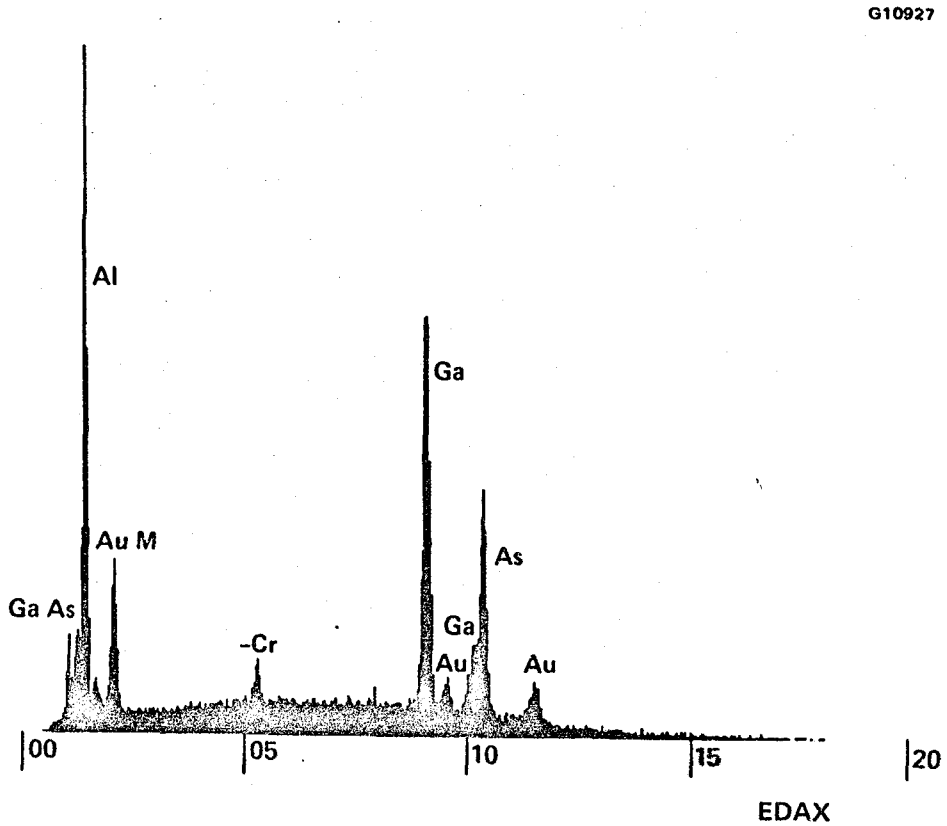


Figure B-4 X-ray analysis of channel.

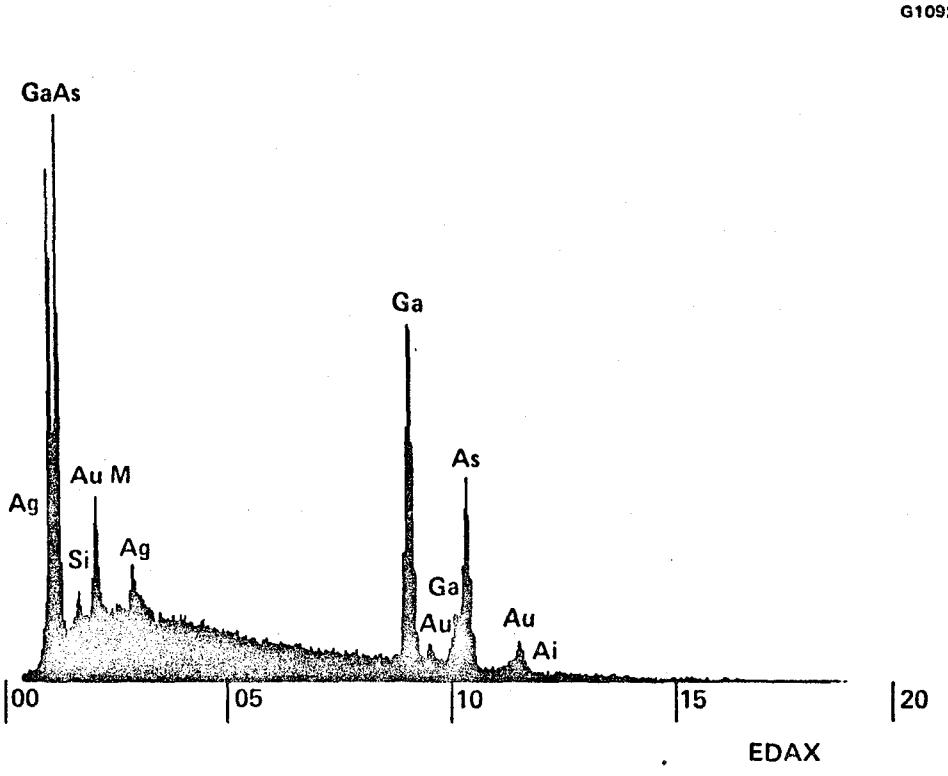


Figure B-5 X-ray analysis of chip surface.

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